A BATTERY HARVESTING BUCK-BOOST CONVERTER USING DUAL PATH OPERATION FOR INDUCTOR CURRENT REDUCTION

Trung Kien Vu[1], Xuan Canh Pham[2], Xuan Thanh Pham[1,*]

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ABSTRACT

Being able to accommodate varying power supply while maintaining a stable output has became a standard for DC-DC converters. This article introduces a dual conduction paths buck-boost converter at reducing inductor current stress and conduction losses by having an additional path for current to traverse as well as having only one power switch in series with the inductor. Through simulations, the efficiency of the converter with respect to output current. In Buck mode, the efficiency remains high at around 96.7% at low current levels and gradually decreases as the current increases, but stays above 96% up to 1 A. In contrast, the Boost mode starts with an efficiency of about 91% and gradually increases with higher current, reaching approximately 95% at 1 A.

Keywords: *DC-DC converter, buck-boost converter.*

[1]School of Electrical and Electronic Engineering, Hanoi University of industry, Vietnam

[2]Faculty of Electronics, Telecommunications and Technical reconnaissance, People's Police University of Technology and Logistics, Vietnam

[*]Email: thanhpx@haui.edu.vn

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1. INTRODUCTION

Recent developments in the field of physics and materials have led to a spurred of lithium-based battery in IoT and portable devices due to their ability to hold great energy while taking up minimal spaces [1]. But these batteries also suffer from physical degradation, over time, they have shown case a gradual decrease in output voltage, typical lithium battery can have an output voltage ranging from 4.2 to 2.7V [2]. In order to increase battery lifetime and achieve load regulations, the implemented power converter must ensure stability and high efficiency within all of the given voltage range of the battery [3]. Given such requirements of power converters, buck-boost converters are usually employed [4, 5]. However, the conventional buck-boost converter experience extensive conduction losses due to having two power switches in series with the inductor on the main current path. Also, a minimum dc resistance and high saturation current is required from an inductor to accommodate for large inductor current in a conventional design, forcing the use of larger inductor which cause integration issues regarding sizing components. To address the problem above, the design [6] used flying capacitors only act as a voltage source during boost stage to bypass a power switch in the main current path and reducing conduction losses but that also resulted in a voltage stress [7]. Another solution was presented in [8], but such hybrid switch-capacitor based designs with extensive utilization of switches will introduce more switching losses and reduce energy density [9]. Therefore, we propose a buck-boost converter that uses dual-path configuration for both boost and buck operation for inductor current reduction in both operation which results in reduced losses and improving overall efficiency while not exposing power switches to voltage stress. The article is organized as follows: Section 2 will explain the designs and implementations and the results and conclusions will be available in section 3 and 4, respectively.

2. DESIGN

The overall system of the circuit and the proposed dual-path buck-boost converter are both shown in Fig. 1. The entirety of the circuit consists of the proposed converter which generate the desired V_{OUT} of 3.4V in both operation mode which is then compared by a folded cascode amplifier to a reference voltage V_{REF} to amplify the mismatch between the feedback voltage and the required output and create our error voltage V_{EA}. V_{EA} is

then feed into a common source stage referenced to a sawtooth signal coming from the ramp generator. A mode selector is utilized to determine whether the voltage need to be boosted or step-down by comparing the input voltage V_{IN} with V_{REF} and the results will be forwarded to logic controls circuit along with the amplified difference between our V_{EA} and ramp signal after being fed through an SR-FF to generate a baseline control clock signal. The control logics will output clock signals into bootstraps, level shifts and buffers to drive four power switches $S_{1\div4}$ in the power stage.

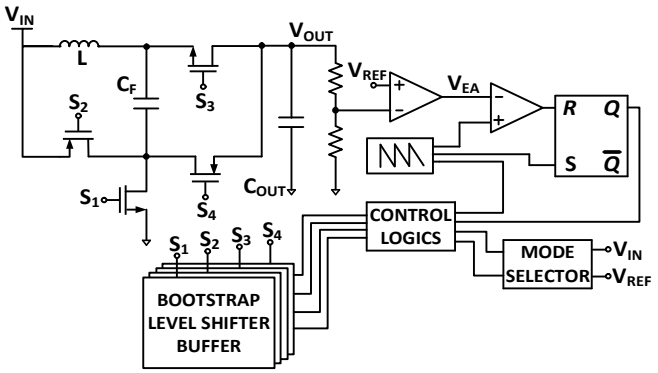


Fig. 1. Overall system

Unlike conventional buck-boost design, the proposed converter utilized a flying capacitor C_F in parallel with the inductor, hence the name "dual-path", to reduce the inductor current in all phases of operations. As mentioned, the proposed converter works in Boost Mode and Buck Mode, and is split into four different phases. The converter enters phase 1 and 2 repeatedly during Boost Mode at $V_{IN} < V_{OUT}$ whereas phase 3 and 4 is used in Buck Mode when $V_{IN} > V_{OUT}$. The detailed operations of the four phases are shown in Fig. 2. During Boost Mode, the converter enter phase 1 and start to soft charging C_F, due to an inductor voltage-second balance ensuring the average voltage across an inductor is zero in a complete switching cycle we can derive that:

$$D(V_{IN}-(V_{OUT}-V_{IN}))=(1-D)(V_{OUT}-V_{IN}) \quad (1)$$

From equation (1), the conversion rate (CR) is determined as:

$$M=\frac{V_{OUT}}{V_{IN}}=1+D \quad (2)$$

While the amount of electric charge supplied by the inductor in one period is:

$$I_L(1-D)T+I_L DT=MI_L T \quad (3)$$

Plugging the M term from equation (2) into (3) we have:

$$I_L=\frac{MI_{OUT}}{1+D} \quad (4)$$

In Buck Mode operation, the converter first enters phase 3 where the inductor is being charged with a value equal V_{IN}-V_{OUT} whereas in phase 4 it has a voltage of V_{IN} - $2V_{OUT}$ and supplying charge to C_F, then CR is expressed as follows:

$$M=\frac{V_{OUT}}{V_{IN}}=\frac{1}{2-D} \quad (5)$$

From: $$D(V_{IN}-V_{OUT})=(1-D)(V_{IN}-2V_{OUT}) \quad (6)$$

With the same amount of charge sending to load as in equation (3), plug in term M from equation (5) we arrived at:

$$I_L=\frac{1}{2-D}I_{OUT} \quad (7)$$

with the additional derivation of equation (4), it is concluded as the inductor current has been reduced in both operations compared to a conventional design (when M > 1).

In the converter, S_1 functions as an NMOS transistor governed by V_{IN}, but S_2 and S_4 operate as PMOS transistors regulated by both V_{IN} and V_{OUT}. In boost mode, the switching node V_{SW2} alternates between V_{IN} and 0, with the body of S_4 connected to V_{OUT}. In buck

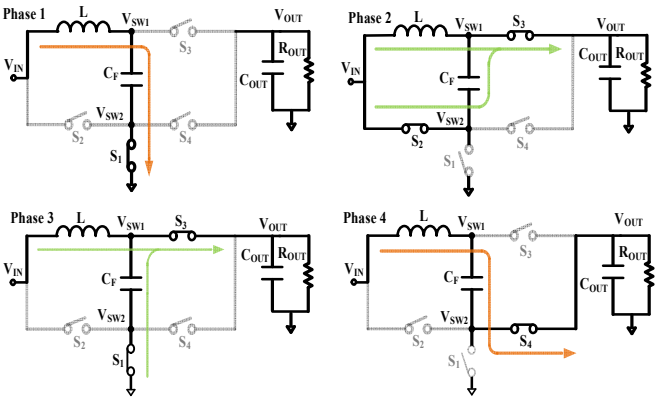
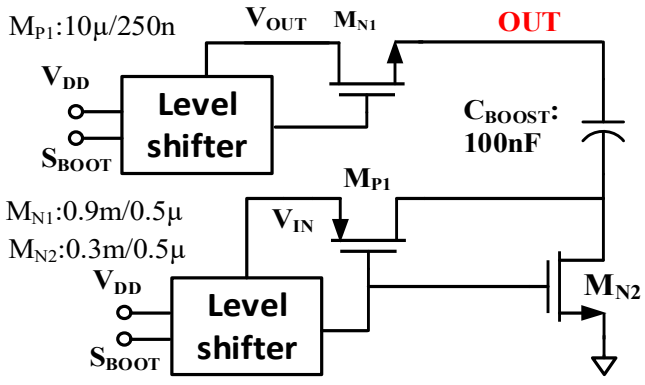


Fig. 2. Phases of operations

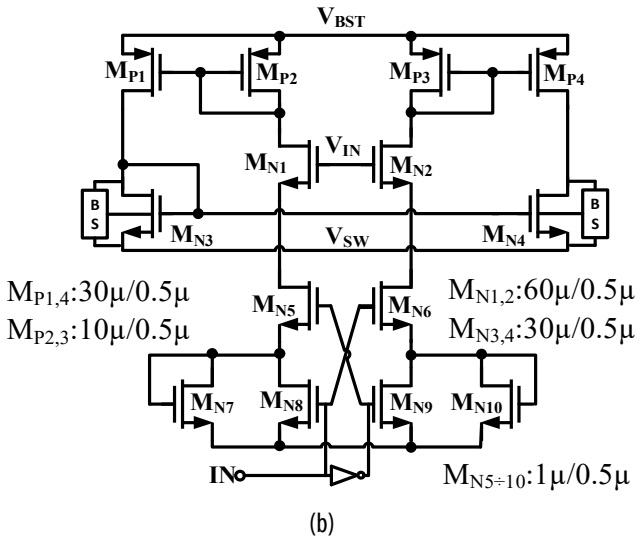
mode, V_{SW2} fluctuates between V_{OUT} and 0, with $S_{2's}$ body linked to V_{IN}. Switch S_3 employs an NMOS transistor to enhance area efficiency in high RMS current conditions. In boost mode, V_{SW1} alternates between V_{OUT} and (V_{OUT} - V_{IN}), which is less than V_{OUT}. In buck mode, V_{SW1} alternates between V_{OUT} and $2V_{OUT}$, the latter being greater than V_{OUT}. A distinct body switch circuit is employed to guarantee proper body terminal connection. This circuit adaptively alters $S_{3's}$ body connection, enabling it to rapidly track the lower

potential between V_{SW} and V_{OUT} in each mode, hence enhancing switching performance and overall efficiency. To operate S_3 effectively, a bootstrap circuit depicted in Fig. 3(a) and a level shifter illustrated in Fig. 3(b) are employed. The bootstrap voltage (V_{BST}) oscillates between V_{OUT} and $V_{OUT} + V_{IN}$, guaranteeing adequate gate drive for S_3 in both operational states. In boost mode ($V_{IN} < V_{OUT}$), S_3 activates during Phase 2 and deactivates during Phase 1. In Phase 1, the boot-strap capacitor (C_{BOOST}) charges to V_{OUT}; subsequently, in Phase 2, it charges to $V_{OUT} + V_{IN}$, supplying sufficient gate drive voltage. In buck mode ($V_{IN} > V_{OUT}$), S_3 activates during Phase 3 and deactivates during Phase 4. In this scenario, C_{BOOST} charges to V_{OUT} during Phase 4 and subsequently to $V_{OUT} + V_{IN}$ in Phase 3, ensur-ing stable operation. V_{SW} serves as the ground reference for the S_3 driver, hence streamlining the gate driver design. In Phase 4, V_{SW} surpasses V_{BST}, attaining $2V_{OUT}$, which is comparable to V_{OUT}. To prevent the level shifter (V_{S3}) output from inadvertently being charged to $2V_{OUT}$ through the body diode of the NMOS transistors (M_{N3}, M_{N4}), a body-switching technique is employed on M_{N3} and M_{N4}. This technique guarantees that when the level shifter input is "1," V_{S3} remains at V_{BST}, regardless of whether V_{BST} is less than V_{SW}. This design eliminates unwanted conduction pathways, ensuring reliable and efficient switching operation of S_3 in both buck and boost modes. In Fig. 3(b), IN denotes the control signal for S_3.

The mode selection circuit is engineered to dynamically alternate between working modes in the proposed converter, minimizing both conduction and switching losses while prolonging battery life to enhance overall efficiency. The converter functions in buck mode when the supply voltage (IN1, the signal fol-lowing the voltage divider of V_{IN}) exceeds both V_{BUCK} = 1.2V and V_{BOOST} = 1V, hence facilitating efficient step-down conversion.



(a)



(b)

Fig. 3. a) Bootstrap schematic; b) Level Shifter schematic

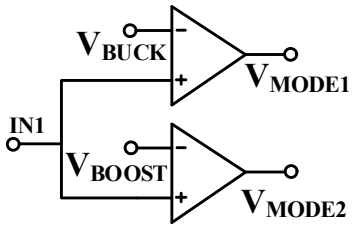


Fig. 4. Mode-select circuit

Conversely, when the supply voltage (IN1) falls below V_{BOOST}, the system activates boost mode, enabling the output voltage to be adjusted appropriately. Given that the system functions with a 1.8V power supply, a voltage divider circuit is employed to appropriately scale V_{IN} prior to processing, so assuring compatibility with the internal control logic. In buck mode, when IN1 exceeds V_{BUCK} and IN1 exceeds V_{BOOST}, the mode selector outputs V_{MODE1} = 1 and V_{MODE2} = 1, signifying buck operation. In boost mode, when IN1 is less than V_{BOOST}, the mode selector establishes V_{MODE1} = 0 and V_{MODE2} = 0, initiating boost conversion. The mode selector is essential for optimizing power efficiency and stable operation by regulating the transition between different modes.

3. RESULTS

The proposed converter is designed using 180nm CMOS process. The power stage utilized a relatively low switching frequency of 1MHz in order to minimize switching losses in the power MOSFETs, while also integrating a 2.2µH inductor, one 4.7µF flying capacitor, one 10 µF output capacitor, and one 100 nF boot-strap capacitor. The converter has efficiently harvested battery energy from a wide range of input voltage from 2.7 - 4.2V as discussed. Illustrated in Fig. 5, the efficiency of the

converter with respect to output current. In Buck mode, the efficiency remains high at around 96.7% at low current levels and gradually decreases as the current increases, but stays above 96% up to 1A. In contrast, the Boost mode starts with an efficiency of about 91% and gradually increases with higher current, reaching approximately 95% at 1A. This indicates that Buck mode performs more efficiently at lower currents, while Boost mode shows significant improvement in efficiency as the current rises.

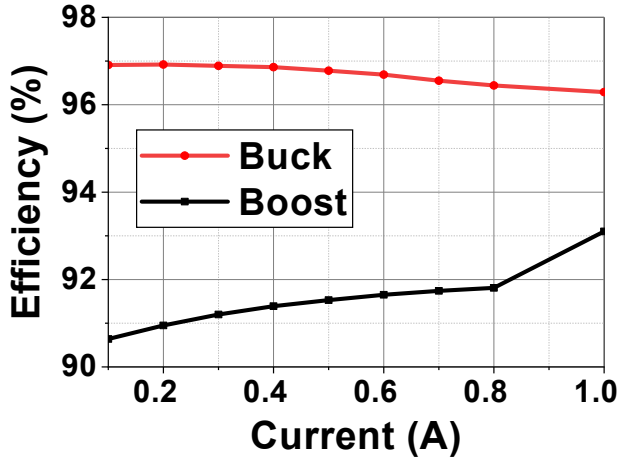


Fig. 5. Efficiency of the converter in both operation modes

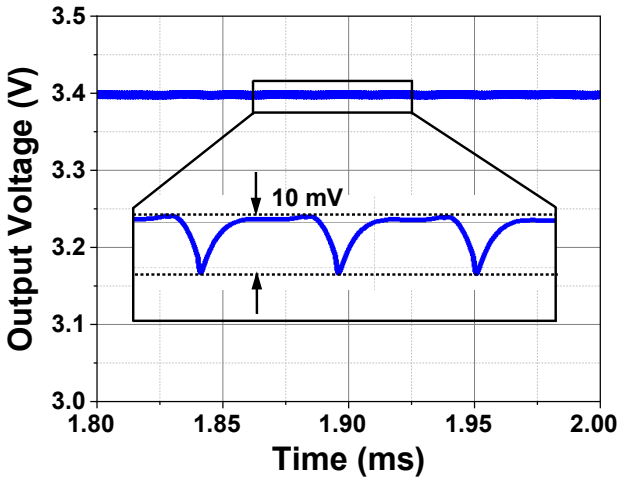


Fig. 6. Output voltage and ripples during Buck Mode

Fig. 6 and Fig. 7 illustrate the output voltage as a function of time in a power converter circuit, with an enlarged section highlighting the ripple voltage, respectively. Fig. 6 illustrates the converter functioning in Buck mode, maintaining a steady output voltage of 3.4V and a ripple voltage of 10mV, indicating reduced noise and enhanced filtering efficacy. Fig. 7 illustrates the converter functioning in Boost mode, which sustains the output voltage at 3.4V; nevertheless, it exhibits an elevated ripple voltage of 20mV, leading to increased fluctuation compared to Buck mode. In both modes, the ripple voltage remains below 1% of the output voltage, demonstrating effective voltage regulation and stable performance.

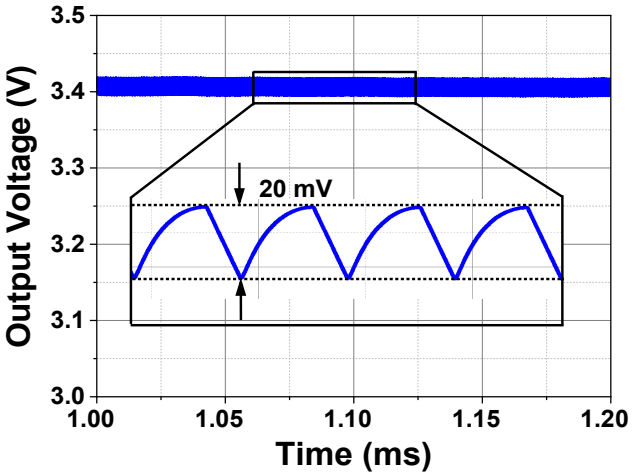


Fig. 7. Output voltage and ripples during Boost Mode

4. CONCLUSION

This paper delineates a hybrid buck-boost converter employing merely four switches and a single flying capacitor. A notable benefit of this design is that all power switches exhibit resilience to voltage stress issues. By using dual-path operation in both buck and boost modes, the converter substantially decreases inductor current across the entire battery voltage range. Moreover, the converter achieves a maximum efficiency of approximately 96%.

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