# A DESIGN OF LOW NOISE 10-BIT ENOB 57.9dB SNDR SAR ADC USING MODULATION COMPARATOR

## THIẾT KẾ SAR ADC 10-BIT ENOB 57,9dB SNDR CÓ ĐỘ NHIỄU THẤP SỬ DỤNG BỘ SO SÁNH ĐIỀU CHẾ

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**ABSTRACT**

This article presents a design of low noise 10-bit Effective Number of Bits (ENoB) 57.9dB Signal-to-noise and distortion ratio (SNDR) Successive approximation-register (SAR) Analog-to-digital converter (ADC) using modulation comparator, suitable for modern biomedical applications. In this design, a Two-stage Op-amp Modulation (TOM) has been applied, which consists of a two-stage op-amp combined with two synchronized polarity-reversing choppers. Although 1/f noise and mismatch effect have been significantly reduced by using two-stage op-amp with modulation technique, there are still some limitations. In particular, modulation technique is imperfect, combined with offsets caused during the manufacturing process, will cause output ripple leading to low output signal quality. To overcome this, a compensation technique using two-stage Double Cross Integrator Amplifier (DCIA) are applied in the proposed ADC to optimize comparator performance, minimize offset and noise. Using 180nm CMOS technology, the proposed SAR ADC needs a 0.55mm$^2$ active area. With a power of 2.135mW and a Figure-of-Merits (FoMs) of 0.37 pJ/step.conv. In addition, the proposed SAR ADC achieves a Signal-to-noise ratio (SNR) of 56.40dB, a SNDR of 57.9dB, and a Signal-to-noise ratio and distortion (SINAD) of 56.40dB. Furthermore, this work attains an ENoB of 9.08-bit.

***Keywords:*** *Successive approximation-register Analog-to-digital Converter; Two-stage Op-amp Modulation; two-stage Doubled Cross Integrator Amplifier; modulation technique.*

**TÓM TẮT**

Bài báo này trình bày thiết kế của bộ chuyển đổi tương tự sang số (Analog-to-digital converter - ADC) thanh ghi xấp xỉ liên tiếp (Successive approximation-register - SAR) 10-bit số bit hiệu dụng (Effective Number of Bits - ENoB) 57,9dB tỷ lệ tín hiệu trên nhiễu và méo (Signal-to-noise and distortion ratio - SNDR) có độ nhiễu thấp sử dụng bộ so sánh điều chế, phù hợp cho các ứng dụng y sinh hiện đại. Trong thiết kế này, cấu trúc mạch khuếch đại hai tầng điều chế (Two-stage Op-amp Modulation - TOM) đã được sử dụng, bao gồm mạch khuếch đại hai tầng kết hợp với hai chopper đảo ngược cực đồng bộ. Mặc dù nhiễu 1/f và sự mismatch đã được giảm đáng kể bằng cách sử dụng mạch khuếch đại hai tầng với kỹ thuật điều chế, nhưng vẫn còn một số hạn chế. Cụ thể, kỹ thuật điều chế không hoàn hảo, kết hợp với sự mismatch phát sinh trong quá trình sản xuất, sẽ gây ra gợn sóng đầu ra dẫn đến chất lượng tín hiệu đầu ra thấp. Để khắc phục điều này, một kỹ thuật bù trừ sử dụng bộ tích phân ghép chéo khuếch đại hai tầng (Double Cross Integrator Amplifier - DCIA) được áp dụng trong ADC được đề xuất để tối ưu hóa hiệu suất của bộ so sánh, giảm thiểu sai số đầu ra và nhiễu. Sử dụng công nghệ CMOS 180nm, ADC SAR được đề xuất có diện tích hoạt động 0,55mm$^2$. Với công suất 2,135mW và tham số đánh giá hiệu năng (Figure-of-Merits - FoM$_S$) là 0,37 pJ/step.conv. Ngoài ra, ADC SAR được đề xuất đạt tỷ lệ tín hiệu trên nhiễu (Signal-to-noise ratio - SNR) là 56,40dB, SNDR là 57,9dB và tín hiệu tạp âm và méo (Signal-to-noise ratio and distortion - SINAD) là 56,40dB. Hơn thế nữa, bài báo còn đạt được ENoB là 9,08-bit.

***Từ khóa:*** *Bộ chuyển đổi tương tự sang số thanh ghi xấp xỉ liên tiếp; mạch khuếch đại điều chế hai tầng; bộ tích phân ghép chéo khuếch đại hai tầng; kỹ thuật điều chế.*

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**SYMBOL**

| Symbol | Unit | Meaning |
|---|---|---|
| ENoB | bit | Number of effective bits |
| SNDR | dB | Signal-to-noise ratio and distortion |
| SNR | dB | Signal to noise ratio |
| FoMs | pJ/step.conv | Performance evaluation parameters |
| SINAD | dB | Signal noise and distortion |
| $V_{REF}$ | V | Reference voltage |
| VCM | V | General voltage |
| Cunit | F | Capacitance |
| Noise | mV/sqrt Hz | Noise |

**ABBREVIATIONS**

| | |
|---|---|
| ADC | Analog-to-Digital Converter |
| SAR | Successive Approximation-Register |
| ENoB | Effective Number of Bits |
| SNDR | Signal-to-Noise and Distortion Ratio |
| SNR | Signal-to-Noise Ratio |
| FoMs | Figure-of-Merits |
| SINAD | Signal-to-Noise ratio And Distortion |
| CMOS | Complementary Metal-Oxide-Semiconductor |
| TOM | Two-stage Op-amp Modulation |
| DCIA | two-stage Double Cross Integrator Amplifier |
| ECG | Electrocardiogram |
| S/H | Sample and hold |
| DAC | Digital-to-Analog Converter |
| COMP | Comparator |
| DEC | Decoder |
| MSB | Most Significant Bit |
| LSB | Least Significant Bit |
| FC | Folded-cascode |
| CS | Common source |
| CMFB | Common mode Feedback |
| CLK | Clock |
| D-FF | Data Flip-Flop |
| TG | Transmission-Gate |
| FFT | Fast Fourier Transform |
| IRN | Input-Referred Noise |
| W/L | Width/Length |

## 1. INTRODUCTION

Nowadays, people's demand for both health and life is increasing with the continuous development of technology [1, 2], so the application of digital solutions in the biomedical field is becoming more and more important, especially in the use of electrocardiogram (ECG) sensors [3]. In fact, some medical devices, such as heart rate monitors, health monitors,… still do not meet hardware standards to optimize the use and analysis of data from ECG sensors [4]. For example, some current devices can only read and process analog signal data from sensors and cannot take full advantage of the capabilities of digital technology. To improve this problem, speed and accuracy in identifying and processing signals from ECG sensors must be a top priority. SAR ADC, an indispensable part of modern medical devices, plays an important role in signal recognition and processing, responsible for converting analog signals from sensors into digital data that computers and other digital devices can process it [5]. To achieve the best performance, SAR ADC often operates at the resolution range from 8 bits to 14 bits. The performance of the SAR ADC largely determines the speed and accuracy of data processing from the ECG sensor.

An indispensable component in many biomedical and biosensor systems, comparators compare voltage values, check for errors, measure and test, and control system quality [6]. In SAR ADC, the comparator plays an extremely important role, because of the ability to accurately convert small analog signals into digital data. The speed, accuracy, noise and offset of the comparator significantly affect the performance of the ADC. There are two common types of comparator including dynamic latch and two-stage op-amp. The dynamic latch comparator [7] is becoming more and more popular because of its high comparison speed and low power consumption. However, dynamic latch comparators are not suitable for applications that need to process large or complex data due to disadvantages such as low stability, generation of kickback noise, and limited scalability. In this paper, the proposed two-stage op-amp is used to overcome the shortcomings of dynamic latch comparator, but at the cost of high input impedance and offset [8]. To overcome these drawbacks, the compensation technique combined with the input impedance increase technique is used in the comparator. In this, capacitors are attached to the output of the amplifier to calibrate the output signal. Furthermore, the positive feedback loop consists of a logic circuit and a

feedback capacitor is added to take advantage of voltage compensation to optimize the input impedance. Although this method may expand the operating area as well as consume more power, improving comparator performance is an important future task.

Using 180nm CMOS technology, the proposed SAR ADC needs a 0.55mm$^2$ active area. With a power of 2.135mW and a Figure-of-Merits (FoMs) of 0.37 pJ/step.conv. In addition, the proposed SAR ADC achieves a Signal-to-noise ratio (SNR) of 56.40dB, a Signal-to-noise and distortion ratio (SNDR) of 57.9dB, and a Signal-to-noise ratio and distortion (SINAD) of 56.40dB. Furthermore, it attains an Effective Number of Bits (ENoB) of 9.08-bit.

## 2. COMPARATOR ARCHITECTURE

SAR ADC is a type of ADC that converts continuous analog signal into discrete digital signal [9]. The basic schematic structure of 10-bit SAR ADC is presented in Fig. 1. consisting of the following blocks: Sample and hold (S/H), Comparator, SAR logic, and Digital-to-analog Converter (DAC). The S/H circuit is crucial for accurately converting the analog input signal to a digital output by sampling and holding the input sample. Next, the digital signal voltage value at the output of S/H will be detected and compared with the output voltage of DAC by comparator. The output of the comparator depends on whether the input voltage is greater or lesser than the output voltage of DAC. When the conversion process begins, the SAR sets the Most Significant Bit (MSB) to 1 and the remaining bits to 0. Therefore, the DAC input value will be 1000000000 leading to the DAC generating a voltage equal to half the $V_{REF}$, which will be compared with the input voltage and based on the output of comparator, the output of the SAR logic will be adjusted continuously. This process will be repeated until all bits in the SAR are determined.

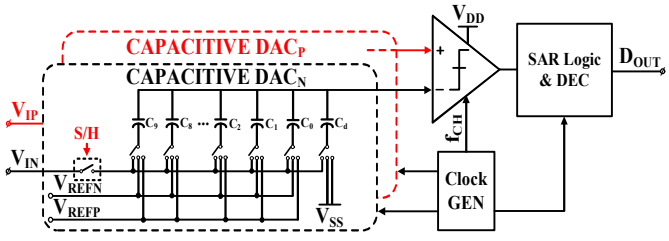



Fig. 1. Schematic of propose 10-bit SAR ADC

To increase accuracy, reduce noise and offset in the ADC, TOM structure with offset auto compensate open loop is applied in the comparator as shown in Fig. 2. Adding another loop from the input of $G_{m1}$ to the output of the TOM consisting of two choppers and an amplifier in between is an optimal way, but this increases power consumption and creates additional ripple at the output. As an alternative, the comparator with chopper uses offset auto compensate open loop, which consists of DCIA to minimize $V_{OS}$, includes amplifier $G_{m3}$, resistor $R_{int1,2}$, and capacitor $C_{int1,2}$ = 1pF, as shown in Fig. 3. First, after being modulated through $CH_{in}$, the input difference of DCIA is $V_{OS}$, at this time the two inputs will have the values $V_{in1} = V_{in} + V_{OS}$ and $V_{in2} = V_{in}$ respectively. To minimize offset, the input will first be dumped to the branch DCIA to balance voltage.

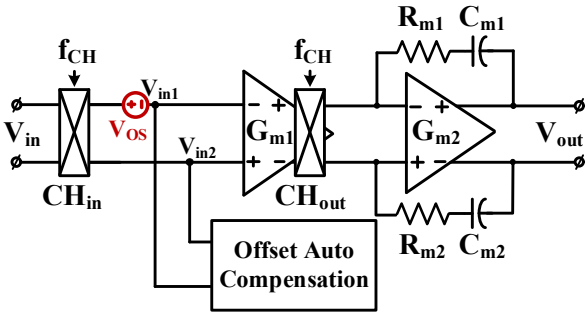



Fig. 2. Schematic of comparator using chopper with $C_{m1,2}$ = 1pF

Specifically, after being amplified through $G_{m3}$, $V_{in1}$ is fed back into $V_{in2}$ and $V_{in2}$ is also fed back into $V_{in1}$, at this time the two inputs of $G_{m1}$ have been voltage balanced $V_{in1} = V_{in2} = V_{in} + V_{OS}$. Therefore, the DCIA uses feedback cross-compensation technique to minimize $V_{OS}$ leading to reduced output ripple.

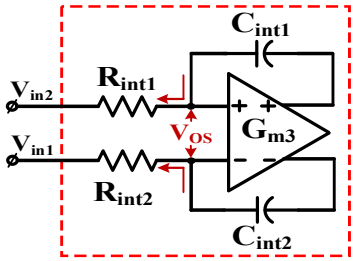



Fig. 3. Schematic of offset auto compensation open loop using DCIA structure

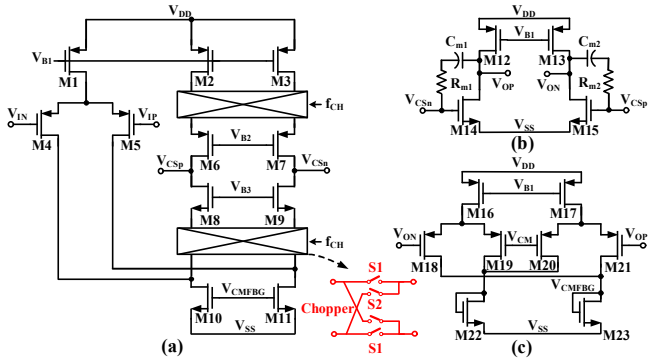



Fig. 4. Schematic of the (a) folder-cascode amplifier using chopper ($G_{m1}$); (b) common source stage and (c) common-mode feedback circuit ($G_{m2}$)

The first stage of TOM, namely $G_{m1}$, using Folded-cascode (FC) structure is a two-stage differential amplifier commonly used in integrated circuit design, shown in Fig. 4a. This circuit is symmetrically configured with an additional input stage and the second stage is a cascode stage. Due to the use of multiple pairs of stacked symmetrical transistors (cascode circuit) combined with the folder circuit, the FC achieves high gain, high output impedance, and wide bandwidth. However, the use of many transistors increases the mismatch combined with the unevenness of the input (the difference between $V_{IN}$ and $V_{IP}$) causing the offset voltage phenomenon, which leads to the appearance of output ripple affecting the amplification efficiency of the circuit. To overcome this, the chopper technique is applied to the FC circuit to reduce the offset voltage. Specifically, in Fig. 4a, when the CLK pulse with frequency $f_{CH}$ acts on the choppers at a high level, the $S_1$ switch pair turns off, $S_2$ turns on causing the current from $M_2$ and $M_3$ to flow down to $M_7$ and $M_6$, while $M_8$ and $M_9$ flow down to $M_{11}$ and $M_{10}$. This creates cross-coupled transistors that balance the current difference between transistors (due to mismatch and input voltage difference), thereby reducing offset and output ripple of the amplifier circuit. Next, the output of the FC stage is connected to the input of the second stage ($G_{m2}$) using a Common-Source (CS) amplifier, shown in Fig. 4b. When the CS amplifier circuit operates, the voltage between input and output changes, so Miller capacitors ($C_{m1,2}$) and resistors $R_{m1,2}$ are used to store and release energy based on the change. This change balances phase and frequency to improve the stability of the entire circuit. In addition, a Common-mode feedback (CMFB) circuit is also attached in the two-stage amplifier circuit to help adjust the common output voltage level to the $V_{CM}$ level, shown in Fig. 4c.

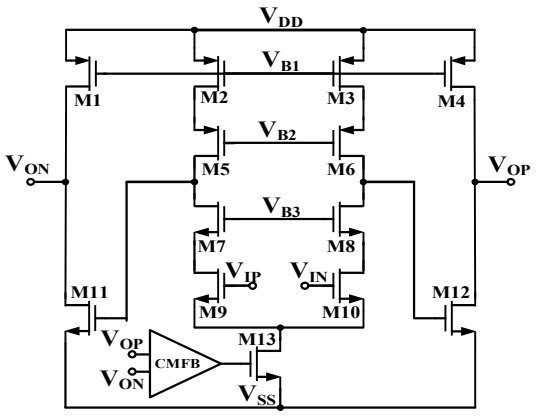



Fig. 5. Schematic of the telescopic amplifier with common source stage and common-mode feedback circuit ($G_{m3}$)

Table 1. Parameters of $G_{m1}$, $G_{m2}$ and $G_{m3}$

| $G_{m1}$ | | $G_{m2}$ | | $G_{m3}$ | |
|---|---|---|---|---|---|
| **Parameter** | **W/L (µm)** | **Parameter** | **W/L (µm)** | **Parameter** | **W/L (µm)** |
| $M_1$ | 30/0.7 | $M_{12}$, $M_{13}$ | 15/0.7 | $M_1$, $M_2$, $M_3$, $M_4$, $M_5$, $M_6$ | 15/0.7 |
| $M_2$, $M_3$, $M_4$, $M_5$, $M_6$, $M_7$ | 15/0.7 | $M_{14}$, $M_{15}$ | 0.7/0.7 | $M_7$, $M_8$, $M_9$, $M_{10}$ | 8/0.7 |
| $M_8$, $M_9$, $M_{10}$, $M_{11}$ | 8/0.7 | $M_{16}$, $M_{17}$, $M_{18}$, $M_{19}$, $M_{20}$, $M_{21}$ | 15/0.7 | $M_{11}$, $M_{12}$ | 0.7/0.7 |
| | | $M_{22}$, $M_{23}$ | 8.5/3 | $M_{13}$ | 8/2 |

The schematic of the two-stage op-amp ($G_{m3}$) is shown in Fig. 5 using a Telescopic amplifier circuit structure combined with common source (CS) and common-mode feedback (CMFB). With a symmetric-transistors stacked structure, the Telescopic has high gain, good stability and is capable of amplifying to the maximum level of the source. The second amplifier stage uses a Miller-compensated CS amplifier circuit to increase gain and phase stability. Additionally, a CMFB is also added to regulate the common-mode output voltage to reach the $V_{CM}$ level. The W/L parameters of the transistors are presented in Table 1.

## 3. SAR ADC 10-BIT OPERATION

### 3.1. DAC

Digital-to-Analog Converter (DAC) is an important component in the ADC shown in Fig. 1. The DAC converts the digital value into a voltage or current level proportional to the voltage referent. The DAC is made up of two symmetrical capacitor arrays, each array consists of a binary weighted capacitor bank and a dummy capacitor. Dummy capacitors do not participate in the conversion process but help balance voltage and charge in the circuit, reduce quantum noise and increase stability by charging and discharging electricity. The proposed DAC with two capacitor arrays uses the power redistribution method on the capacitors, which improves the performance of the DAC compared to the capacitor arrays structure thank to better noise rejection from common-mode rejection.

### 3.2. SAR logic

The SAR logic in SAR ADC functions according to the binary search principle, which involves multiple D flip-flop logics (D-FF) as presented in Fig. 6. When the conversion process begins, the MSB is set to 1, while the other bits are set to 0.

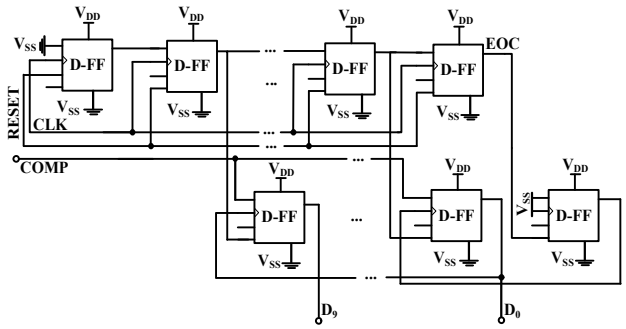



Fig. 6. Structure of SAR logic 10-bit

This value is then converted to an analog signal by the DAC and compared with the analog input signal. If the DAC signal is smaller than the input signal, the MSB bit is left unchanged. Otherwise, the MSB bit is set to 0. This process is then repeated for each subsequent bit in the register, from MSB to Least Significant Bit (LSB). Once all the bits have been processed, the final value in the SAR logic is the digital representation of the input analog signal.

### 3.3. S/H

The sample and hold (S/H) circuit in a SAR ADC is Transmission-Gate (TG-switch), which samples and stabilizes the analog signal during conversion [10]. This improves conversion accuracy by ensuring that the analog signal value does not change. In the proposed SAR ADC, the Bootstrap circuit shown in Fig. 7, is used to reduce noise, increase conversion speed and be more stable when compared to traditional TG-Switch. On the other hand, the circuit design becomes more complicated as well as consumes more power because the Bootstrap circuit requires additional components and complex control circuits.

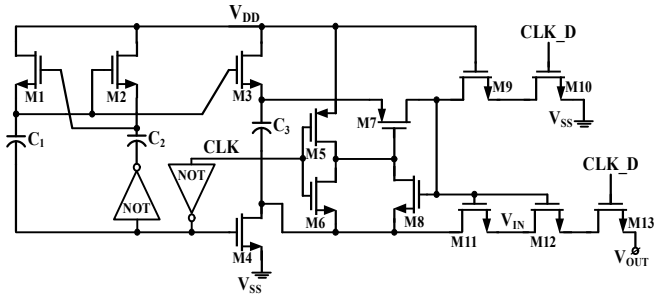



Fig. 7. Structure of bootstrap in the proposed SAR ADC

## 4. RESULTS AND DISCUSSION

Using 180nm CMOS technology, the proposed SAR ADC needs a 0.55mm$^2$ active area, the layout of this design is shown in Figure 8a. Featuring a power consumption of 2.135mW in Fig. 8b. Furthermore, the suggested SAR ADC attains an SNR of 56.40dB, an SNDR of 57.9dB and SINAD of 56.40dB. Moreover, the expected SAR ADC achieves FFT-response at 1.66mV as in Fig. 9b and Fig. 9a shows the floorplan of DAC. Regarding to 1/f noise measure in Fig. 10a, comparator without chopping technique reach 141.3mV/sqrt Hz, while comparator with chopping is lower, at 100.466mV/sqrt Hz.

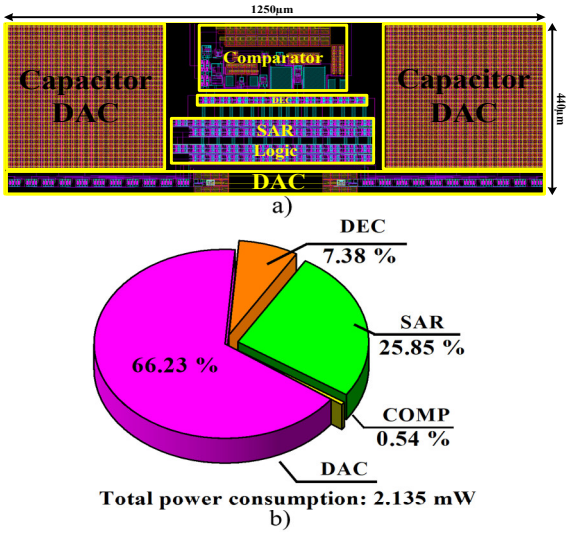



Fig. 8. a) Layout of the SAR ADC 10-bit; b) Total power consumption of proposed SAR ADC

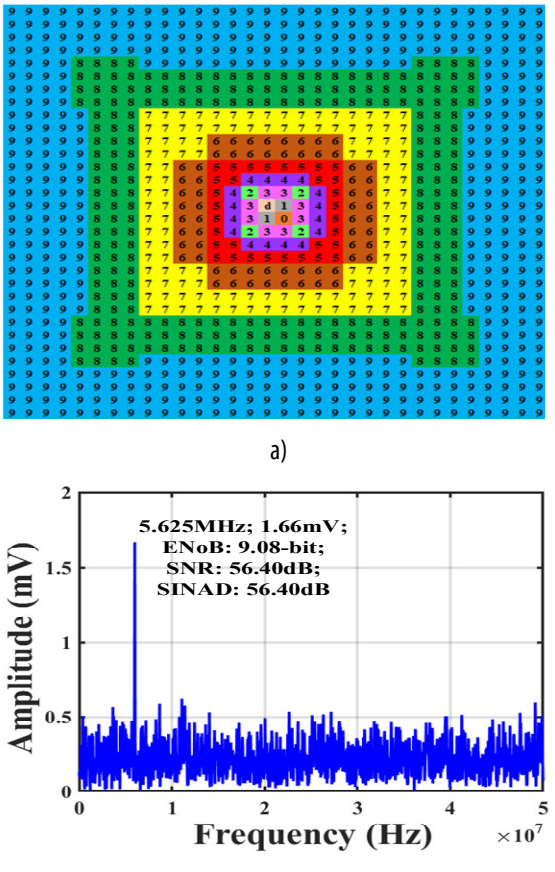
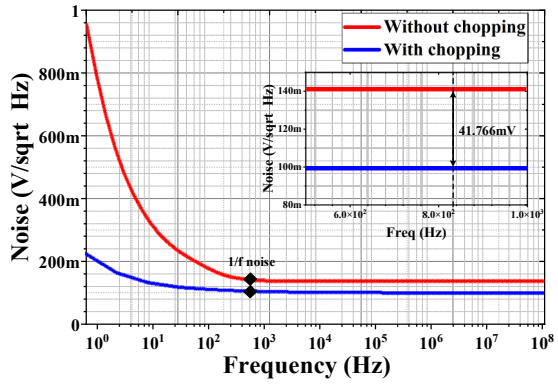
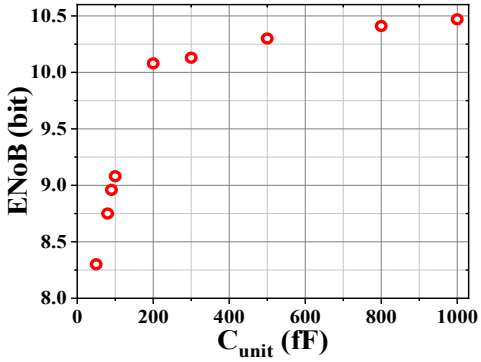



Fig. 9. a) The floorplan of DAC; b) FFT-response in proposed SAR ADC 10-bit




a)




b)

Fig. 10. a) The 1/f noise measurement of comparator with/without chopping; b) the ENoB measurement of proposed SAR ADC

Fig. 10b shows the ENoB levels with different $C_{unit}$ in a distribution chart. From 0 to 100fF, the ENoB gradually increases from approximately 8.3 to 9.08-bit at 100fF. Besides, ENoB has a jump from 9.08-bit to 10.08-bit (higher than proposed ENoB) when $C_{unit}$ increases to 200fF, which has a negative effect on output quality. Therefore, an ENoB of 9.08-bit with a $C_{unit}$ of 100fF is recommended to choose in this work. To improve SNDR, increasing the resolution along with ENoB is often the top priority. However, rising ENoB leads to a higher capacitor value, causing kT/C noise that affects the overall performance of the SAR ADC. In addition, a larger capacitor value also results in a larger required area and higher power consumption. Therefore, designing an ADC to achieve a ideal SNDR level is not always feasible or efficient.

Table 2. The comparison of measured performance

| Parameter | [11] | [12] | [13] | [14] | This work |
|---|---|---|---|---|---|
| Tech. (nm) | 130 | 180 | 130 | 180 | 180 |
| Architecture | Chopper-LNA | CCCIA | DCCS | CSMUL | DCIA |
| Supply (V) | 1.2 | 1.6 | 1.2 | 1.8 | 1.8 |
| Frequency (Hz) | 250K | 85.9 | 130 | 1-100 | 5.625M |
| Resolution (bits) | 18 | 10 | 8 | 12 | 10 |
| ENoB (bits) | 14.4 | 9.64 | 6.7 | 11.02 | 9.08 |
| SNDR (dB) | 88.2 | 59.8 | 44.5 | 75.68 | 57.9 |
| SFDR (dB) | 94.4 | - | 56.5 | - | 77.09 |
| IRN (V/√Hz) | 2.52μ | 0.645μ | 4.2μ | - | 10.36f |
| Power (μW) | 5.5m | 85 | 9.1 | 2,560 | 2,135 |
| Area ($mm^2$) | 4 | 3.81 | 16 | 8.6 | 0.55 |

DCCS: Direct-coupled chopper-stabilized; CSMUL: Chopper-stabilized Multipath.

Finally, Table 2 compares the performance of proposed SAR ADC in this paper to others. Table 2 presents a comparison with other previous works. Using 1.8-V voltage supply and the highest $F_{in}$ is 5.625MHz, this proposal achieves a higher ENoB compared to similar works, at 9.08-bit. With less power consumption and low IRN, this work is especially suitable for biomedical applications needing extended battery life and highly accurate sensors.

## 5. CONCLUSION

In this article, a 10-bit SAR ADC using a converter simulated with 180nm CMOS technology is presented. The proposed comparator in the SAR ADC uses a two-stage DCIA open-loop structure, achieving certain goals, including low offset, low 1/f noise, and high stability, but in return, it has a large area, complex circuit structure, and high power consumption. This contributes to the development of electrocardiogram sensor technology, opening up a new step for the biomedical industry worldwide.

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