A 2-PHASE HYBRID BOOST CONVERTER WITH SHARED BOOTSTRAP CAPACITOR ACHIEVING 90% EFFICIENCY AT 5.0 CONVERSION RATE

THIẾT KẾ BỘ CHUYỂN ĐỔI NÂNG ÁP 2 PHA CẤU TRÚC LAI CÙNG VỚI MẠCH BOOTSTRAP SỬ DỤNG CHUNG TỤ ĐẠT HIỆU SUẤT 90% TẠI HỆ SỐ CHUYỂN ĐỔI 5.0

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ABSTRACT

Many devices now require a higher voltage supply than its predecessors. This has enabled the development of hybrid boost topology, which proved to have a higher conversion rate, though not without its own problems, especially the hard-charging of capacitors. This work introduces a voltage converter that eliminates hard-charging losses by ensuring that the flying capacitors charge and discharge through inductors. The design is simulated in the Cadence 180nm CMOS process. The step-up power conversion from the input voltage of 2 - 4.2V to 15 - 20V output voltage, providing 1.3 - 5W output power at 2MHz operating frequency. The simulation result shows a peak efficiency of 90% at 3.3V input voltage and 16.5V output voltage.

Keywords: *DC-DC converter, 2-phase hybrid boost, soft charging, capacitor cross-connected, shared capacitor bootstrap.*

TÓM TẮT

Nhiều thiết bị hiện nay yêu cầu nguồn điện áp cao hơn so với các thiết bị đời trước. Xu hướng này đã tạo điều kiện cho sự phát triển của mạch chuyển đổi nâng áp cấu trúc lai, được chứng minh là có tỷ lệ chuyển đổi cao hơn so với mạch nâng áp truyền thống, mặc dù vậy, cấu trúc lai tồn lại những vấn đề riêng cần được khắc phục, đặc biệt là vấn đề về sạc cứng trên các tụ điện. Đề tài này nghiên cứu và thiết kế một bộ chuyển đổi điện áp giúp loại bỏ tổn thất do sạc cứng bằng cách đảm bảo rằng các tụ điện được sạc và xả qua các cuộn cảm. Thiết kế của bộ chuyển đổi được mô phỏng bằng phần mềm thiết kế vi mạch Cadence 180nm CMOS. Bộ chuyển đổi nâng áp hoạt động với điện áp đầu vào 2 - 4,2V và cung cấp điện áp đầu ra 15 - 20V, công suất đầu ra đạt 1,3 - 5W ở tần số hoạt động 2MHz. Kết quả mô phỏng cho thấy hiệu suất cực đại đạt 90% ở điện áp đầu vào 3,3V và điện áp đầu ra 16,5V.

Từ khóa: *Bộ chuyển đổi DC-DC, mạch nâng áp 2 pha cấu trúc lai, sạc mềm, tụ điện mắc chéo, mạch bootstrap sử dụng chung tụ.*

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SYMBOL

Symbol	Unit	Meaning
V_G	V	Pulse controls the power transistor
V_S	V	pulse control does not pass through the bootstrap
I	mA	Current
V	V	Voltage
ΔI	mA	Current ripple
ΔV	mV	Voltage ripple
f_{SW}	MHz	Switching frequency
T_{SW}	µs	Operating cycle
T_{ON}	µs	Inductor charging time

T_{OFF}	µs	Inductor discharge time
L	H	Inductance
C	F	Capacitance

ABBREVIATIONS

DC	Directional Current
IoT	Interner of Things
SoC	System-on-a-Chip
RMS	Root mean square
ESR	Equivalent Series Resistance
DSD	Double-step-down
CCC	Capacitor Cross-Connected
CMOS	Complementary Metal-Oxide-Semiconductor
CR	Conversion Rate
NMOS	N-channel Metal-Oxide-Semiconductor
D	Duty cycle
PWM	Pulse Width Modulation
CLK	Clock

1. INTRODUCTION

Currently, system on chip (SoC) serves as an essential technology for small mobile systems that consume little energy, such as Internet of things (IoT) devices, smartphones [1, 2]. Multiphase DC-DC converter is implemented to lower input current ripple and increases output current [3] by equally splitting delivered current to each phase. However, control signals and inductors mismatches caused current imbalance, inducing a higher current stress on specific phases leads to lowered output current, higher ripple and RMS current loss, overall degrading components quality. The previous works [4-6] proposed solution by implementing current sensor circuits and balancing control schemes, requiring additional power consumption and increase complexity. Additionally, conventional boost converter with a high step-up output voltage suffers from high voltage stress on power transistors [7], which need high-voltage processes resulting in increased silicon area and cost overhead, also parasitic capacitance. Therefore, flying capacitors was implemented to stack up voltage, but capacitor hard-charging causes ESR loss [8, 9]. As explained in [10], soft-charging operation requires capacitor charging and discharging through a current source, or an inductor, exclusively. Moreover, conventional boost converters face issues with gate control signal pulse width (T_{OFF}). A sufficiently long T_{OFF} is required for gate drive and feedback loop propagation, resulting in a longer T_S (switching period), increased I_L, and the need for larger inductors due to limited operating frequency. To extend the pulse width without compromising performance, double-step-down (DSD) topologies provide a solution [8], though it has a higher output current ripple compared to traditional boost converters. In this paper, a two-phase flying capacitor cross-connected (CCC) boost converter is presented, having a high CR and power density. It effectively eliminated C_F hard-charging, narrow pulse width, and output current ripple issues. More details are presented in subsequent sections.

2. PROPOSED DESIGN OF 2-PHASE HYBRID BOOST CONVERTER

Fig. 1 shows the proposed variation of Switched Capacitors topology for Boost Converter, more specifically a newly introduced 2-Phase Hybrid structure. For details, the circuit presented a 2-Phase Hybrid Boost Converter mentioned above which is practically a conventional 2-Phase Boost Converter that use NMOS exclusively but also having a little twist of containing a pair of cross-connected capacitors along with a pair of inductors which differentiated the work from conventional Switched Capacitors architecture, hence the name "hybrid". With the problem of inductor currents ripple as mentioned above, we exploited the factor of having multiple phases in order to implement two different inductors for each phase which means the ΔI_L will cancel each other out and effectively reduce the currents ripple.

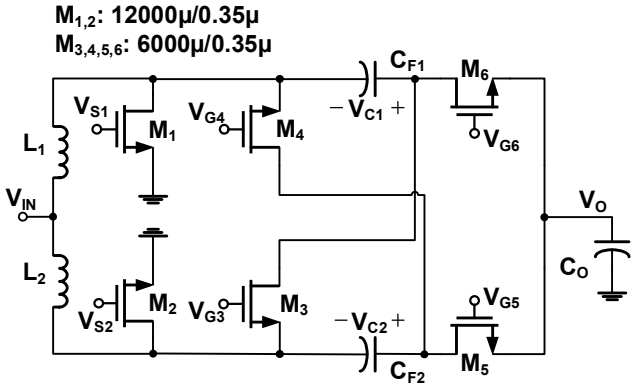


Fig. 1. 2-Phase Hybrid Boost Converter

Fig. 2 shows the circuit's operations with two distinct phases, each phase can be broken down into state 1-3. In state 1, M_1, M_3, and M_5 are turned on, grounding inductor L_1 and allowing it to charge. Simultaneously, L_2 discharges through two flying capacitors, C_{F1} and C_{F2}, due to the activation of switches M_3 and M_5. M_1 connects C_{F1}

to the ground, causing its voltage level to rise to $V_{OUT}/2$, while C_{F2} discharges to supply our load. In state 2, a similar process occurs, but M_2, M_4, and M_6 are active instead, L_1 is discharged while L_2 is charged through C_{F1} and C_{F2} via switches M_4 and M_6. M_2 connects C_{F2} to the ground, raising its voltage to $V_{OUT}/2$, and C_{F1} discharges to the load. In state 3, both M_1 and M_2 are turned on while the rest of the switches (M_3-M_6) are turned off. This configuration effectively shorts both inductors to the ground through M_1 and M_2, allowing them to maintain the charge between C_{F1} and C_{F2} while charging them in preparation for the next iteration of the operating circle. Two operating phases, phase 1 and phase 2, create an iterative loop operates sequentially from phase 1 (state 1 → state 3) → phase 2 (state 2 → state 3) → phase 1 (state 1 → state 3) and so on. This operating scheme minimizes current ripples while providing a continuous output current during both state 1 and state 2, enhancing the overall efficiency and performance.

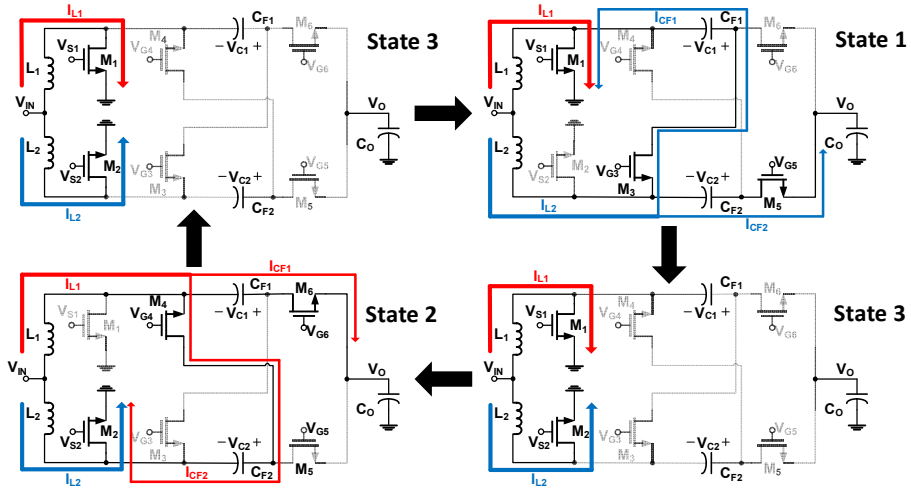


Fig. 2. Steady-state operation of the converter

Each inductor is charged by shorting to ground in DT_{SW} and discharged through two flying capacitors in $(1 - D)T_{SW}$. Voltage that is generated by the inductor in a discharge period equal to $V_{IN}/(1 - D)$, charging a flying capacitor being shorted to ground. Storing a voltage of $V_{IN}/(1 - D)$ on the flying capacitor, in the next period, the other inductor worked as the same and applying a voltage of $V_{IN}/(1 - D)$ on the opposite terminal of the flying capacitor, thus, a voltage equals to $2{\cdot}V_{IN}/(1 - D)$ is delivered to output, in turns deriving a conversion ratio:

$$CR = \frac{2}{1-D} \quad (1)$$

that double the conversion ratio compared to conventional 2-Phase Boost converter. Additionally, higher output voltage means the voltage stress will be a major problem if not dealt with correctly. Table 1 provide an overview on voltages stress across all six NMOSs.

Table 1. Voltage stress on switches

State	M_1	M_2	M_3	M_4	M_5	M_6
1	0	$V_O/2$	0	V_O	0	$V_O/2$
2	$V_O/2$	0	V_O	0	$V_O/2$	0
3	0	0	$V_O/2$	$V_O/2$	$V_O/2$	$V_O/2$

As observed, V_{DS3} and V_{DS4} became V_O in state 2 and 1, respectively while having a stress of $V_O/2$ at state 3 but with the rest of our switches only experience a voltage of $V_O/2$. Thus, low V_{DS} ratings devices can be implemented for M_1, M_2, M_5, M_6 for reducing in both the required silicon area and the parasitic capacitance while in theory still use higher V_{DS} ratings devices for M_3, M_4 in order to maintain the circuit's operation integrity which is a problem we can easily bypass with using the same devices as M_1, M_2, M_5, M_6 but with an increase in quantity and connect them in parallel.

I_L on each phase and V_{CF} on its opposite phase have a dependency relation to each other. That relation will ensure the balance of inductors currents even when we take the possibilities of differences in inductors, capacitors values and gate driving signals, thus eliminating the need for complex control schemes in order to manage the imbalanced currents and ensuring the reliability of the circuit.

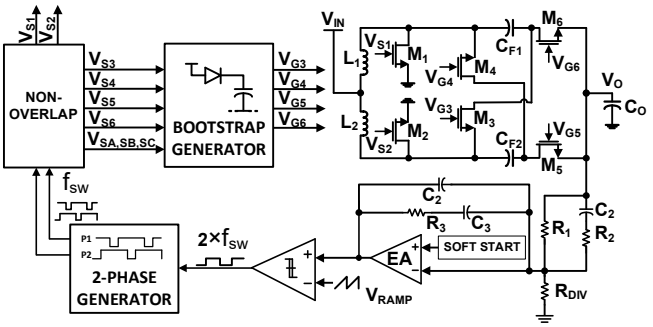


Fig. 3. Voltage mode control loop

For precise voltage regulation, a control feedback loop is implemented. Output voltage V_O is fed to inverting input of error amplifier for negative response, while non-inverting input is set to a reference voltage V_{REF}. Controlled by a voltage mode scheme, a type 3

compensation network is implemented for stability and transient response. The difference between error amplifier's inverting input (V_{FB}) and non-inverting input (V_{REF}) is amplified and compared to a sawtooth wave-form V_{RAMP} working at $2\times f_{SW}$ by the comparator, generating a $2\times f_{SW}$ PWM signal. By using a digital logic circuit, 2-phase control signal is generated, working at f_{SW} frequency. Duty cycle time period applied to power stage can be calculated from PWM signal's duty cycle by:

$$D = \frac{1 + D_{PWM}}{2} \quad (2)$$

indicates that, the lowest operating duty cycle is D = 0.5 when $D_{PWM} = 0$.

To prevent shoot through between M_1 and M_4 (M_3 and M_2), a non-overlapping circuit is needed.

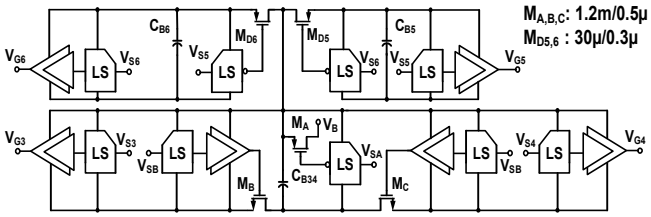


Fig. 4. Gate-drive circuit with shared bootstrap capacitor scheme

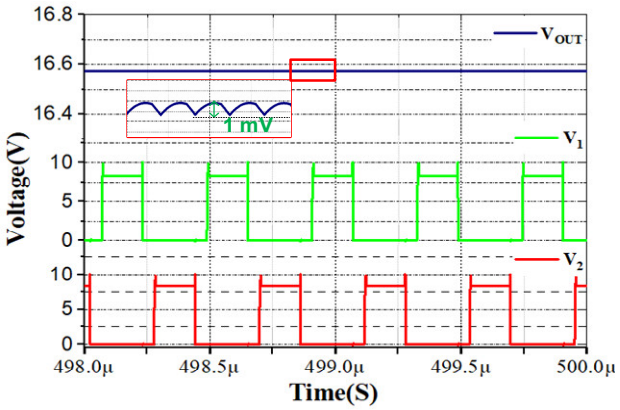
In this work, certain NMOS switches shown in Fig. 4, including M_3, M_4, M_5, and M_6, require bootstrap voltage due to their floating sources, which is crucial for properly operating. A typical bootstrap circuit comprises of a bootstrap capacitor (C_{BOOT}), a voltage source providing charge to the bootstrap capacitors (V_{BOOT}), and the NMOS's source voltage (V_S). The gate-source voltage (V_{GS}) generated by the bootstrap circuit is essentially the difference between V_{BOOT} and V_S when V_S is at a low level. To optimize efficiency and minimize component quantity, the operation timing of M_3, M_4, M_5, and M_6 can be leverage. These switches operate at different time intervals, thus allowing us to implement a shared bootstrap capacitor, C_{B34}, which reduces the overall area required for bootstrap capacitors. Furthermore, there is a need for different voltage levels of V_{BOOT} for M_3 and M_5 (and M_4 and M_6) due to differences in their source voltage levels. However, a single shared voltage source, $V_{C,B34}$, operating at a high level, can effectively charge both C_{B5} and C_{B6}. This approach simplifies the bootstrap circuitry while maintaining the necessary voltage levels for proper gate driving. By employing the shared bootstrap capacitor and voltage source strategy, we achieve efficient gate driving for the NMOS switches in a streamlined and area-efficient manner.

3. SIMULATION RESULTS

In this paper, a 2-Phase Hybrid Boost converter is simulated. For small size and reducing inductor current ripple, 3.3µH inductors is used. Owing to Capacitor Cross-Connected (CCC) implementation, flying capacitors values can be reduced to 470nF, a 10µF output capacitor is implemented to filter out the output voltage ripple.

Fig. 5(a) shows steady-state waveforms at V_{IN} = 3.3V, CR = 5, I_{OUT} = 97mA. As observed, output voltage is regulated with output voltage error about 2.43%. Output voltage ripple $\Delta V_O \approx$ 1mV is detected which smaller than single-phase boost converter owing to interleaved inductor currents. V_1 and V_2 represent voltage stress on M1, M2 switching between 0 and $V_O/2$ is halved by implementation of flying capacitors.

Fig. 5(b) illustrates input current waveform I_{IN} and inductor current waveforms I_{L1} and I_{L2}. As observed, input current ripple ΔI_{IN} is reduced due to the cancellation between I_{L1} ripple and I_{L2} ripple which reduces RMS input current as a benefit of multiphase configuration.



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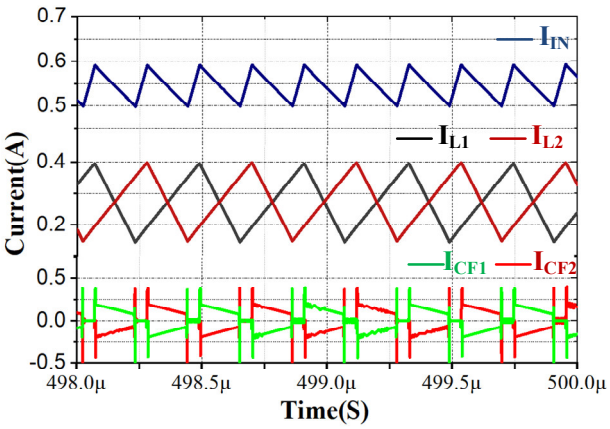
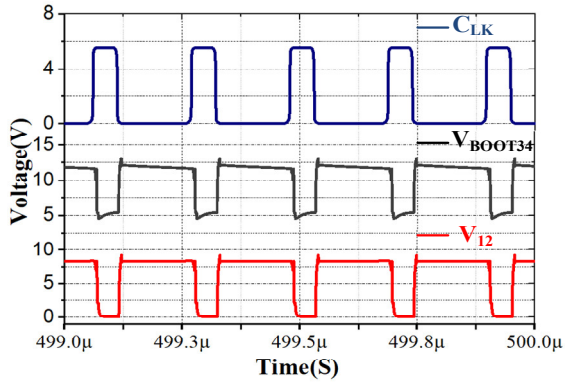


b)

Fig. 5. Measurement of steady-state input currents, inductors currents and flying-capacitor currents waveforms

Fig. 6(a) presents bootstrap voltage waveforms and control clock signal generated from PWM controller. V_{B34} is shifted up by the bootstrap generator with bottom plates voltage is V_{12} which is V_1 and V_2 at high level. For trading-off between size and capacitor gate charge, a 1.2nF bootstrap capacitor is used for C_{B34}, two others bootstrap capacitors C_{B5} and C_{B6} can be smaller are implemented by two 1nF capacitors. A 5.5V external voltage source is needed to charge the main bootstrap capacitor C_{B34}, determining driving gate-source voltage of power switches. Fig. 6(b) shows S_A, S_B, S_C control signal waveforms determining the C_{B34}'s charging and discharging time with V_1 and V_2 as bottom plate voltage, respectively.



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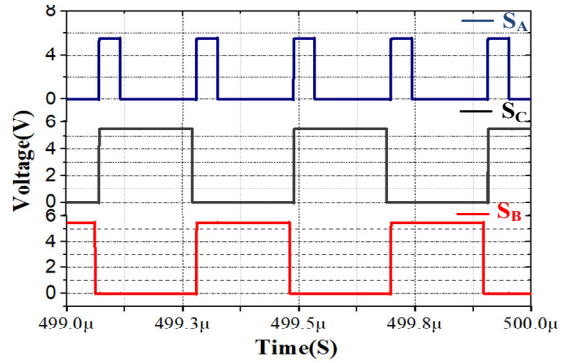
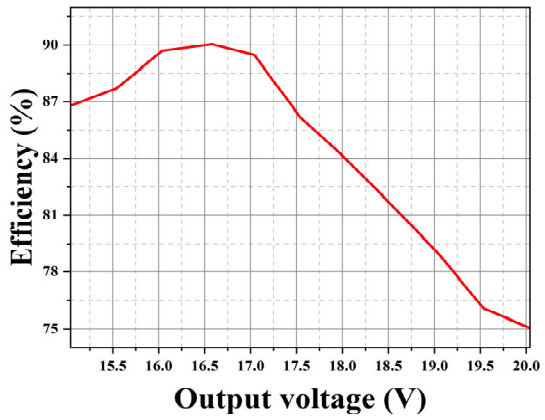


b)

Fig. 6. Measurement result of bootstrap circuit's waveform

Fig. 7(a) shows conversion power efficiency at V_{IN} = 3.3V, output voltage is regulated from 15 - 20V, peak efficiency reaches 90% at conversion ratio CR = 5, corresponding to 16.5V output voltage. Output voltage's transient response is tested by applying stepping load current, simulation result in Fig. 7(b) shows overshoot/undershoot at output voltage approximate 3% compared to regulated output. Table 2 represents comparison this paper with others DC-DC Boost converter topology.



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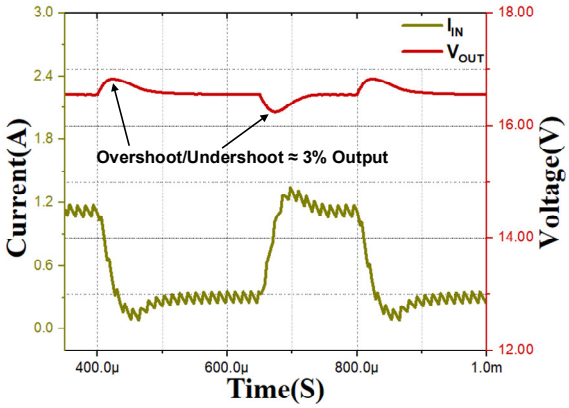

b)

Fig. 7. Efficiency to load impedance

Table 2. Comparison table to other papers

Specifications	This paper	[7]	[8]	[11]
CMOS Process (nm)	180	NA	NA	35
Topology	Hybrid CCC	Conventional	Hybrid	Hybrid
Input voltage (V)	2 - 4.2	4.5 - 27	6 - 18	3.3 - 8
Output Voltage (V)	15 - 20	4.5 - 38	12 - 50	12 - 14.4
Load Current (mA)	8.6 - 250	20 - 120	70 - 100	NA
FSW (MHz)	2	1	0.82	0.5
Multi-Phase	Yes	No	No	Yes
CR	$\frac{2}{1-D}$	$\frac{1}{1-D}$	$\frac{3-D}{1-D}$	
Fly. Cap. (µF)	2×0.47	NA	2x260	
Soft Charging	Yes	NA	No	
Peak Efficiency @ (CR)	90% (CR = 5)	94% (CR = 1.67)	92% (CR = 2.5)	

4. CONCLUSIONS

In this paper, a 2-Phase Hybrid Boost converter is proposed and simulated by using CMOS 180 nm process.

Interleaved inductor currents reduce current ripple, mitigate inductor conduction loss. Cross-connected of flying capacitor is implemented, double pulse width at the same CR compared to conventional Boost converter, reducing switching frequency limitation. Charging and discharging flying capacitor by inductor eliminate hard charging loss.

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THÔNG TIN TÁC GIẢ

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