# DESIGN A LOW POWER, 100dB OPERATIONAL AMPLIFIER USING CMOS TECHNOLOGY

## THIẾT KẾ BỘ KHUẾCH ĐẠI CÔNG SUẤT THẤP, ĐỘ LỢI 100dB SỬ DỤNG CÔNG NGHỆ CMOS

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**ABSTRACT**

The requirement for reduced size and long battery life for portable applications in all based on the conditions has accelerated the trend toward low power silicon chip systems. The supply voltage is being reduced in order to reduce the system's overall power usage. The op-amp (OPA) design for high-speed applications requires proper selection of biasing, logic style and compensation techniques as the technology is scaling down. This paper presents a design of the two-stage op-amps (OPA) using 90nm process with functional verification and gain calculations. In order to improve stability, the compensation technique is added to OPA to improve performance metrics. According to simulation results, the designed OPA obtains a gain of 131dB with 60 degrees phase margin. The OPA achieves a gain-bandwidth (GBW) of 1.26MHz by consuming a current of 2.56μA from a 1.8V supply.

***Keywords:*** *CMOS, op-amp, high gain, low power.*

**TÓM TẮT**

Việc yêu cầu giảm kích thước và kéo dài thời lượng pin cho các ứng dụng di động dựa trên mọi điều kiện đã thúc đẩy xu hướng hướng tới các hệ thống chip silicon sử dụng điện áp và công suất thấp. Điện áp nguồn được giảm xuống để giảm mức sử dụng điện năng tổng thể của hệ thống. Việc thiết kế mạch khuếch đại cho các ứng dụng tốc độ cao đòi hỏi phải lựa chọn đúng xu hướng, lối logic và công nghệ bù khi công nghệ chế tạo đang thu nhỏ. Bài báo này đề cập đến thiết kế của bộ khuếch đại hai tầng sử dụng công nghệ 90nm cho việc kiểm tra hoạt động và tính toán độ lợi. Để mạch hoạt động hiệu quả, kỹ thuật bù được thêm vào mạch khuếch đại để cải thiện các chỉ số hiệu năng. Theo kết quả mô phỏng, mạch khuếch đại được thiết kế với độ lợi 131dB, biên độ pha là $60^0$. OPA đạt được băng thông khuếch đại (GBW) 1,26MHz bằng cách tiêu thụ dòng điện 2,56μA và hoạt động ở điện áp cung cấp 1,8V.

***Từ khóa:*** *MOSFET tích hợp, bộ khuếch đại, độ lợi cao, công suất thấp.*

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### 1. INTRODUCTION

Today's system-on-chip (SOC) applications required the integration of both analog and digital components to address non-functional constraints [1-8]. The best-picked topology can aid with the appropriate design of analog and digital circuits. The topology of the digital circuit components can be chosen. Gates, flip flops, inverters, and amplifiers are examples of digital circuit components. Analog circuit design necessitates a thorough grasp of how the system and the circuit operate [9]. While digital circuitry works with two discrete states, analog circuits deal with continuous values and have numerous parameters to consider. Analog components include switching capacitors, analog-to-digital converters (ADCs), filters, and so on [10-11]. All of these circuit components are aimed at performance metrics like area, speed, noise, gain, power, and so on [12]. Using completely differential circuit ideas and operational amplifiers, low noise, high gain analog components may be constructed Op-Amps.

Op amps are one of the most commonly used building components for analog and mixed signal systems. They are used in anything from DC bias applications to high-speed amplifiers and filters, buffers, summaries, integrators, differentiators, comparators, negative impedance converters, and other uses are all possible with general purpose op-amps [13]. Nowadays, due to the industrial trend of implementing both analog and digital circuits on the same chip, complementary metal-oxide semiconductor (CMOS) technology has surpassed bipolar technology for analog circuit design in a mixed-signal system [14]. While many digital circuits may be modified to a smaller device level with a smaller power supply, most existing analog circuitry requires significant modification, if not redesign, to satisfy the same restrictions. Analog circuits are getting increasingly challenging to enhance when transistor length is reduced to a few tens of nanometers [10].

To satisfy the characteristics and limits, the basic two stage op-amps may be constructed utilizing CMOS technology. Gain, gain bandwidth, slew rate, output-voltage swing, offset, noise, and other fundamental op-amp characteristics are shown below. For a given technology, the open-loop gain of a CMOS-based op-amp cannot equal that of a bipolar-based op-amp. This is due to the low transconductance of CMOS devices as well as the gain decrease caused by channel length modulation effects

in submicron CMOS technologies [11]. As a result, gain boosting strategies must be employed in order to increase the gain. These methods of increasing gain frequently require more intricate circuit topologies and greater power supply voltage which may result in a restricted output voltage swing. As a result, multiple stage amplifiers may be employed to create greater gain in analog circuit designs. However, multistage amplifiers are notoriously difficult to compensate for. There are several compensation algorithms for multistage amplifiers, some of which are similar to those used in general feedback control systems that have been modified for use with electronic amplifiers. Lead-lag networks, pole splitting, layered Miller compensation, and signal level variable components are among the approaches used. Most compensating solutions, however, need a larger circuit area and a more sophisticated design than the dominant pole approach utilized in conventional op-amp construction. The compensation of integrated circuit amplifiers is more challenging than that of discrete component amplifiers due to issues such as a lack of large-sized capacitors, parasitic coupling, and packaging parasitic and on/off chip load concerns [12-14]. The primary goal of this effort is to build a two-stage op-amp with compensating techniques to boost gain, utilizing 90nm technology and a full bespoke design suite from Cadence.

## 2. MATERIALS AND METHODS

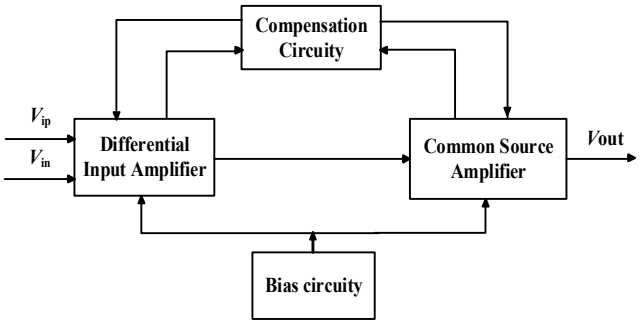


Figure 1. A general two stage of op-amp

Two-stage op-amps mainly consist of cascades of Voltage to Current and Current to Voltages stages. The first stage consists of a differential amplifier that converting the differential input voltage to differential currents [15]. These differential currents are applied to a current mirror load to recover the differential voltage [16-17]. A common source MOSFET converts the second stage input voltage to current in the second stage. This transistor is loaded by a current sink load, which converts the current to voltage at the output. Figure 1 shows the specific two-stage CMOS op-amp. The second step is just the current sink inverter. The second stage of the common source raises the DC gain by an order of magnitude and optimizes the output signal swing for a given voltage supply. This is critical for lower power consumption. If the Op-Amp must drive a low resistance load, the second stage must be followed by a buffer stage whose objective is to lower the output resistance and maintain a large signal swing. A bias circuit is provided to establish the operating point for each transistor in its quiescent stage. To obtain steady closed-loop performance, compensation is necessary.

This paper presents the structure of an analog feedback circuit using a closed-loop circuit to solve the problem of stability and frequency compensation in a linear feedback system-[10]. In order to get stability in the system, in addition to the op-amp circuits, some compensatory techniques are required. There are a number of compensation techniques available such as pole-separated mill compensation, self-compensating capacitors, feed forward compensation using an additional amplifier, negative mill compensation. When compared with other compensation techniques, the compensation technique using a resistor in series with a capacitor and connecting the output signal to the input signal in a second stage provides high gain, high compensation. However, the disadvantage of this structure is that the resistor size is too large, which will increase the size of the chip. This paper uses a C capacitor in series with an N-MOS structure to replace a resistor, still similar to a resistor, but in this structure the resistance value is adjusted by the current source without affecting the current in the second output stage.

Figure 2 shows the proposed two-stage op-amp structure. In two-stage op-amp circuits, the problem often arises due to the pole. Since the two poles dominate the two stages of the op-amp, stability is not guaranteed due to low phase amplitude values. This problem is very dangerous with amplifier circuits, designers need to be careful or else the amplifier will act as an oscillator instead of an amplifier. This structure allows the zero to move out of the right plane causing the zero to disappear so the closed-loop system is stable. Since the current $I_2$ is taken from the voltage supply circuit controlled by the N-MOS and connected in series with $M_2$, the resistance value in $M_2$ is set to a high value. The rate of RC being pushed to the peak but not removed achieves the desired stability.

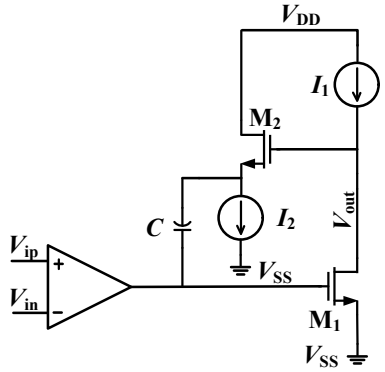


Figure 2. Two-stage op-amp with addition of a source follower to remove the zero

To improve the gain of the amplifier, this paper used the folded cascode structure in the first stage. We found that this structure has a good gain frequency, low power

consumption, large gain and low noise. The second stage uses the NMOS sub-input common source (CS) structure to increase the gain of the op-amp circuit, and at the same time the output DC voltage is adjusted equal to the input DC voltage by the common-mode feedback (CMFB) circuit. Because of the effect of that circuit the output and input DC voltages are balanced.

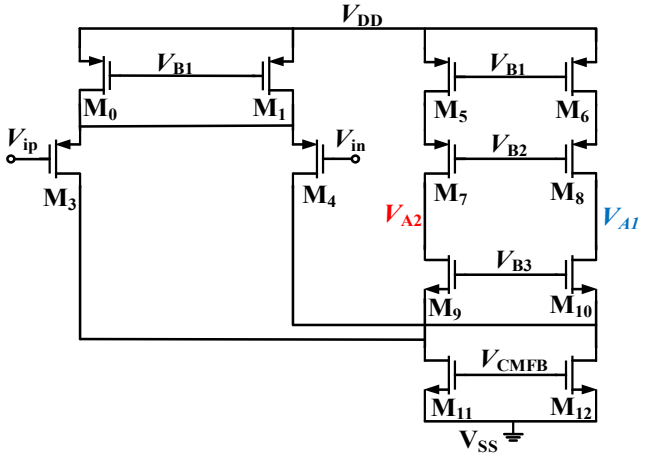


Figure 3. The schematic of the folded cascode stage with PMOS differential input pair

Figure 3 gives a rough depiction of a folding cascode design consisting of a pair of differential inputs $M_3$ and $M_4$ that greatly influence the transconductance's value ($g_m$), followed by a pair of input differentials connected to the common gate stages $M_9$ and $M_{10}$ the full structure current is accumulated at $M_{11}$ and $M_{12}$; because the current source for the whole circuit is supplied to the sub-PMOSs, the CMFB is introduced into $M_{11}$ and $M_{12}$ ($I_{11} = I_{12}$). Transistors $M_{5,6}$, are used to control the current source for each branch so that the resistor value reaches a high value and the current here is set to the lowest level. When the current is reduced, the $R_{out1}$ rises so the circuit's gain increases. Because $g_m$ is proportional to the linearity of the current so the higher the current at $M_0$ and $M_1$, the higher the current passing through $M_3$ and $M_4$ leads to $g_m$ reaching a good value. In order to $R_{out1}$ impedance to increase, the current of $M_5$ and $M_6$ must be lower than the current of $M_{0,1}$. The $R_{out1}$ value is determined by $R_{on} \parallel R_{op}$ where $R_{op}$ is the total resistance value of $M_{5,6,7,8}$ and $R_{on}$ is the total resistance value caused by $M_9$ series with $M_3 \parallel M_{11}$ and $M_{10}$ series with $M_{12} \parallel M_4$. The gain of the first stage is calculated through the formulas (1-3) with $r_o$ being the resistance value tied between D and S in the small signal MOS model in linear.

$$R_{op} \approx g_{m7}.r_{o7}.r_{o5} \quad (1)$$

$$R_{on} \approx g_{m9}.r_{o9}.(r_{o3} \parallel r_{o11}) \quad (2)$$

$$A_{v1} \approx g_{m3}.R_{out1} \approx g_{m3}.(R_{on} \parallel R_{op}) \quad (3)$$

In this paper, the second stage of the op-amp circuit uses a common source structure with two inputs and two outputs. To $g_m$ for the circuit is increased, the power consumption is low, the current through $M_{4,5}$ must be high and current of $I_0 = I_1 = I_4 = I_5$ must be small. Two MOS $M_0$ and $M_1$ create current control resistors for $M_4$ and $M_5$, then the higher the resistor value, the gain of the circuit increases. In the NMOS channel input common source structure, when analyzing the small signal model, the output resistor $R_{out2}$ is determined by the input resistor in parallel with the resistor $r_{0(4,5)}$ in the PMOS. The gain of the second stage is calculated through the formulas in (4-5):

$$R_{out2} \approx r_{o5} \parallel r_{o1} \quad (4)$$

$$A_{v2} \approx g_{m5}.R_{out2} \quad (5)$$

Figure 4 shows that the output signal of the second stage is the input signal of the CMFB block, the $V_{CMFB}$ is put into the first stage so that the DC voltage at $V_{ON}$ and $V_{OP}$ is always approximately 900mV. The $V_{A1}$ and $V_{A2}$ signals on the first stage will be the $V_{IP}$ and $V_{IN}$ inputs of the second stage.

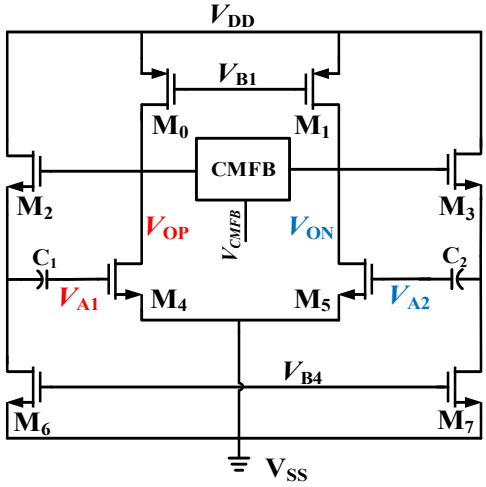


Figure 4. The schematic of output stage with the compensation technique

The voltages $V_{B1}$, $V_{B2}$, $V_{B3}$ and $V_{B4}$ are voltages in the voltage divider that provide equalization of the branches throughout the circuit. The gain of the whole main circuit is equal to the product of the gains of two stages $A_v = A_{v1}.A_{v2}$. From the above formulas, change the size of W and L in each MOS to get the desired both input current and voltage, as well as easily adjust the power consumption of the whole circuit. The Table 1 and Table 2 demonstrate the sizing of CMOS transistors in this paper and the power breakdown of the proposed two-stage.

Table 1. The sizing of CMOS transistors in this paper

| CMOS transistors | The first stage | The second stage |
|---|---|---|
| $M_0$, $M_1$ | 16µm/0.7µm | 8µm/4µm |
| $M_2$, $M_3$ | 18µm/2µm | 12µm/1µm |
| $M_4$, $M_5$ | 8µm/11µm | 8µm/3µm |
| $M_6$, $M_7$ | 8µm/0.7µm | 10µm/3µm |
| $M_8$, $M_9$ | 12µm/1µm | |
| $M_{10}$, $M_{11}$ | 8µm/1µm | |
| $C_1$, $C_2$ | | 10pF |

Table 2. The power breakdown of the proposed two-stage

| Block | Circuit | Components | Current Consumption (µA) |
|---|---|---|---|
| OPA_FC | Folded-Cascode Amplifier | Differential Pair | 1.56 |
| | | Cascode Branches | 0.2 |
| | CMFB | | 0.2 |
| OPA_CS | Common-Source Amplifier | Differential Pair | 0.6 |
| Total | | | 2.56 |

## 3. RESULTS AND DISCUSSION

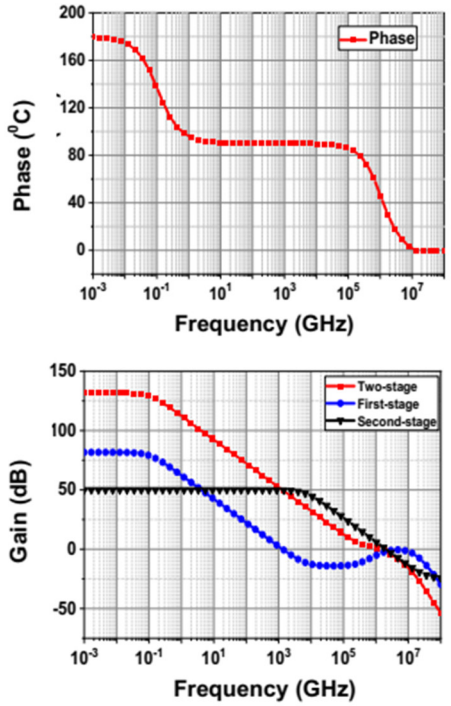


Figure 5. Gain open-loop and phase margin of the two-stage amplifier

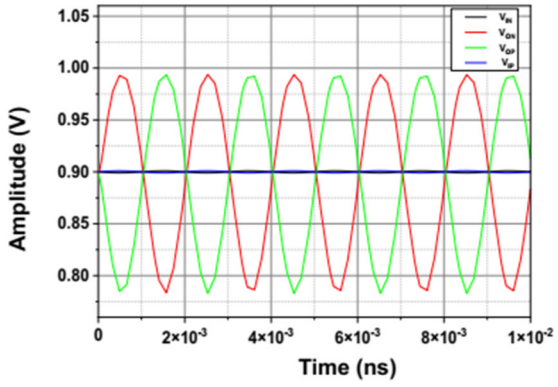


Figure 6. Simulation results closed loop amplifier circuit

The amplifier is fabricated and simulated on 90nm CMOS technology. For the amplifier to work, a voltage bias circuit is required to supply the voltage for the circuit to work. This paper designs a circuit with low power consumption so the current on the two-stage amplifier must be low. A working amplifier circuit requires a voltage bias circuit to supply voltage to the active circuit. In this design, the requirements for good gain, current and phase difference are also achieved. Using the beat tool to simulate the AC analysis, the gain and phase margin of the amplifier are shown in Figure 5. The first stage gain of the folded cascode circuit reaches 80dB, to the second stage the gain of the common source circuit reaches 51dB. Due to the structure of the folded cascode circuit, the current source runs to the first stage, the gain of the first link is higher than the second. The total gain is 131dB and the unified gain bandwidth is 1.26MHz.

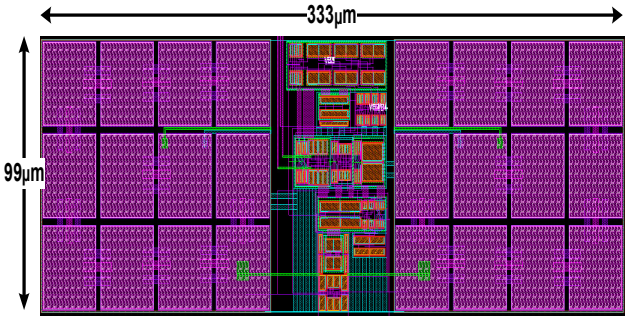


Figure 7. Layout of designed two-stage op-amp with compensation technique

Apply a closed-loop amplifier using capacitive feedback to have $V_{out}/V_{in} \approx C_a/C_x$ where $C_a$ = 5pF, $C_x$ = 50fF with $C_a$, $C_x$ are two load capacitance . Using a transient simulation tool, put two input sinwaves of 500Hz frequency, 1mV amplitude, whose DC voltage origin is approximately 900mV, 180 degrees out of phase to obtain an output signal of the same frequency and amplitude of 999mV. The input-output signal is shown in Figure 6. The op-amp of this paper is fabricated in 90nm CMOS process, the die photograph is shown in Figure 8. The core area is 0.032mm$^2$. Table 3 shows the comparison table of parameters of other architect op-amps.

Table 3. Parameters of other architect op-amps

| Parameter | [18] | [19] | [20] | This work |
|---|---|---|---|---|
| Supply (V) | 1.8 | 1.8 | 3.3 | 1.8 |
| CMOS Technology | 180nm | 180nm | 0.35µm | 90nm |
| Gain (dB) | 70 | 60 | 78 | 131 |
| Phase margin (Degree) | 75 | 63.5 | 63.9 | 60 |
| Power Dissipation (µW) | 19.5 | 37.8 | 144.3 | 4.6 |
| Unity Gain Bandwidth | 8MHz | 5MHz | 1GHz | 1.26MHz |

## 4. CONCLUSION

This paper has proposed a two-stage CMOS op-amp and analyzed its behavior. Simulation results confirm that the proposed design procedure can be utilized to design op-amps that meet all the required specifications. The simulation is done with Cadence software. The design is on 90nm CMOS technology. The unit gain bandwidth achieved for the design is 1.26MHz, the gain is 131dB and phase margin is 60 degrees to ensure a good stability. The total power consumed is 4.6µW.

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**THÔNG TIN TÁC GIẢ**

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