VOLTAGE CONTROLLED RING OSCILLATOR WITH LARGE FREQUENCY RANGE AND VARIABLE DUTY CYCLE

BỘ DAO ĐỘNG VÒNG ĐIỀU KHIỂN BẰNG ĐIỆN ÁP VỚI DẢI TẦN SỐ RỘNG VÀ CÓ THỂ ĐIỀU CHỈNH ĐỘ RỘNG XUNG

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ABSTRACT

Voltage controlled oscillator (VCO) is one of the most important basic blocks for analog, digital as well as in mixed signal circuits. This paper presents a new technique to improve the performance of ring oscillators. A VCO with large tuning range and variable duty cycle is designed using 90nm complementary metal-oxide-semiconductor (CMOS) technology with supply voltage of 1.8Vp-p. The simulation results demonstrate that VCO has high frequency range from 100Hz to 1.77GHz and the duty cycle is adjustable 20% - 80% independent from the oscillation frequency. Simulation results reveal the better performance of the proposed design as compared to existing current starved ring VCO in terms of oscillation frequency and power consumption.

Keywords: *CMOS, voltage -controlled oscillator, ring VCO, large frequency range, variable duty cycle.*

TÓM TẮT

Bộ dao động điều khiển điện áp (VCO) là một trong những khối xây dựng cơ bản quan trọng nhất cho các mạch tương tự, mạch số cũng như các mạch tín hiệu hỗn hợp. Bài báo này trình bày một kỹ thuật mới để cải thiện hiệu suất của bộ dao động vòng. Bộ VCO với dải điều chỉnh tần số lớn và có thể điều chỉnh độ rộng xung được thiết kế bằng công nghệ MOSFET tích hợp với điện áp cung cấp là 1,8V. Kết quả mô phỏng chứng minh rằng bộ VCO có dải tần rộng từ 100Hz tới 1,77GHz và độ rộng xung không phụ thuộc vào tần số dao động có thể điều chỉnh 20% - 80%. Từ kết quả mô phỏng cho thấy hiệu suất của thiết kế được đề xuất tốt hơn so với bộ dao động điều khiển điện áp cơ bản về tần số dao động và điện năng tiêu thụ.

Từ khóa: *CMOS, bộ dao động điều khiển điện áp, bộ dao động điều khiển điện áp vòng, dải tần số rộng, độ rộng xung điều chỉnh được.*

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1. INTRODUCTION

With the advancement of CMOS technology, millions or even billions of transistors may be combined into a single chip, enabling system-on-chip (SOC) architecture. In different types of serial communications, the CPU may need to offer varying data speeds. Moreover, many wireless communication protocols have their unique carrier frequencies. Furthermore, frequency scaling is increasingly critical for low-power operation managers in electronic devices like as computers or mobile phones [1]. As a result, there is little doubt that ring oscillators operating over a wide frequency range are required to achieve those goals.

Designing a voltage-controlled ring oscillator (VCO) with a large frequency range is separate from increasing the driving capability, the loading capacitor, or the number of delay cells [9-10]. The disadvantage of increasing driving capabilities is that it will undoubtedly result in high power consumption. Enlarging the loading capacitor will also take up a lot of die space, and this method is easily influenced by process, voltage, and temperature (PVT) variations [5]. It will also address the issues of high-power consumption and chip space by varying the number of delay stages used to extend the frequency range.

Controlling the resistance is another method for achieving a large frequency range in the voltage-controlled ring oscillator. It creates a better chance to construct a low-power and broad tuning frequency range ring oscillator using a voltage-controlled resistor since it occupies a tiny space and uses no additional power.

The VCO in this paper's proposed is suitable for wireless biotelemetry because of the low power and compact area. So, the concern of low power becomes the key point of the system's requirements. This paper proposed voltage-controlled ring oscillators based on the transmission gate, which is controlled by current and voltage. By adjusting the resistances of the transmission gate, a wide linear tuning frequency range capability can be obtained.

2. CONVENTIONAL CIRCUIT

A ring oscillator made up of several inverter stages, with the output of the final stage feeding back into the first [5]. To oscillate, the ring must have a phase shift of 2π and a voltage gain of unity at the oscillation frequency. Each delay stage must generate an π/N phase shift, where N is the number of delay stages. ADC inversion provides the remaining phase

shift [6]. The delay oscillator is dispersed in the ring oscillator (RO). The ring oscillator has two basic topologies: single-ended and different. The power dissipation of a single-ended topology is computed on a transition basis and has lower phase noise for a given power dissipation. The phase noise differential between these two topologies is higher as the number of steps increases. As a result, the single-ended topology is commonly used. Figure 1 shows the type of single-ended RO.

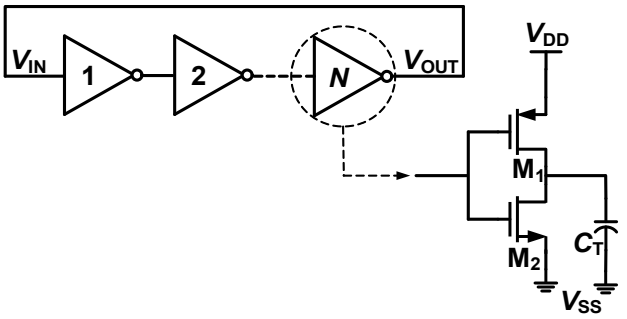

Figure 1. The type of single-end of the basic RO

The oscillator frequency of a standard ring oscillator-based VCO is controlled by varying bias currents. When the bias current is minimal, however, the voltage swing of the VCO becomes slower (long rise/fall time). In some cases, this is undesirable. Furthermore, raising the bias current narrows the voltage headroom of current source MOS transistors. Assume that, each stage provides a delay (t_{DL}). The input signal must pass through N stages, therefore the signal must pass through each N stage once to produce a phase shift initially in $N.t_{DL}$. Then the signal must transit through each phase once again to obtain the remaining phase shift [7]. As a result, the overall cycle or clock is $2.N.t_{DL}$. Here the frequency of the oscillation can be found as the calculator (1).

$$f_{osc} = \frac{1}{2.N.t_{DL}} \quad (1)$$

The difficulty in obtaining a value for the frequency arises when trying to determine t_{DL}, mainly due to the nonlinearities and parasitics of the circuit. As is referred in [8] the delay per stage is defined as the change in output voltage at the midpoint of the transition, V_{SW}, divided by the slew rate, I_{SS}/C_T, resulting in a delay per stage of $C_T.V_{SW}/I_{SS}$. Using definition (1), the oscillation frequency is given by

$$f_{osc} = \frac{I_{SS}}{2.N.V_{SW}.C_T} \quad (2)$$

Figure 2 depicts the fundamental circuit blocks used in this work. In this work, the VCO is made up of three parts: the digital current control circuit, the oscillate circuit, and the circuit duty cycle control. Using transmission gates, the current circuit regulates the input current in the three-stage VCO. V_{CT} is used to control the frequency change. Using a duty cycle circuit consists of two inverters linked in parallel with two inputs, one as the oscillator signal and the other as duty cycle control voltage V_{DT}. Following the transformation, another inverter is applied to purify the signal.

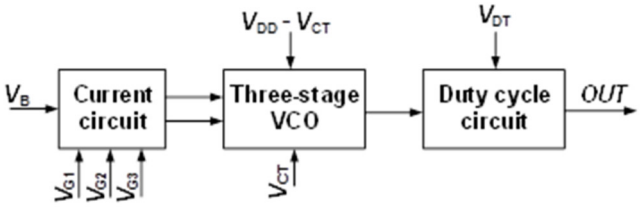

Figure 2. Block diagram of the circuit

2.1. Proposed input current circuit

Figure 3 shows the proposed input current control circuit consisting of four current sources $M_{1,2,4,6}$ biased by a voltage V_B. The transistors $M_{3,5,7}$ is used as switches to control the source current for each branch, respectively $M_{2,4,6}$ by $V_{G1,2,3}$. Next, the current source is fed into M9. Then $M_{10,8}$ copies the current from M_9 and feeds it to the oscillator change the current in the inverter called I_{CTR}.

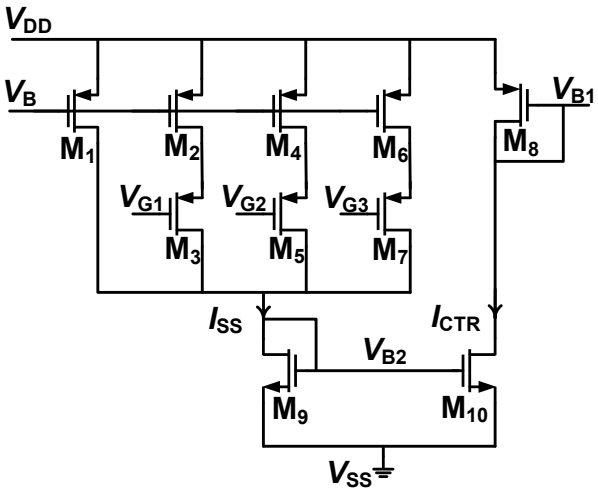

Figure 3. Current control circuit

2.2. Three stage VCO using transmission gates

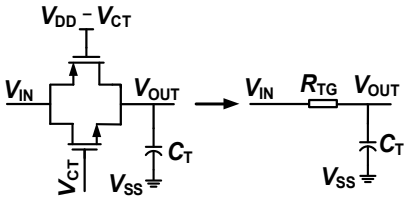

Figure 4. The circuit and equivalent small-signal RC model of transmission gate

The transmission gate (TG), which includes a NMOS and a PMOS transistors connected parallel, is described in Figure 4. The TG is controlled by an external control voltage V_{CT}, hence, the TG operates as a variable resistance. The TG is intended to function as a voltage-controlled switch. When V_{CT} is high, NMOS and PMOS are both biased towards the conduction zone, and the switch closes. The transmission gate's resistance is now quite low. If V_{CT} is low, both MOSFETs are in the cut off area and the switch

operates as an open circuit. In such a circumstance, the resistance must fluctuate substantially depending on the gate voltage.

The circuit scheme is shown in Figure 5. Here a variable resistor R_{TG} is added at the output terminal of each inverter. The delay of each stage t_{DL} can be calculated from the formula (4). Since the MOS transistors in each inverter can be assumed as switches, it can be replaced by a resistance $1/G_M$ in that $G_M = gm_0+gm_1$. Therefore, the delay of each inverter stage t_{DL} and the oscillation frequency are calculated through the formula (5).

$$t_{DL} = \frac{C_T.(1+G_M.R_{TG})}{G_M} \quad (3)$$

$$f_{osc} = \frac{1}{2.N.(\frac{1}{G_M}+R_{TG}).C_T} = \frac{G_M}{2.N.C_T.(1+G_M.R_{TG})} \quad (4)$$

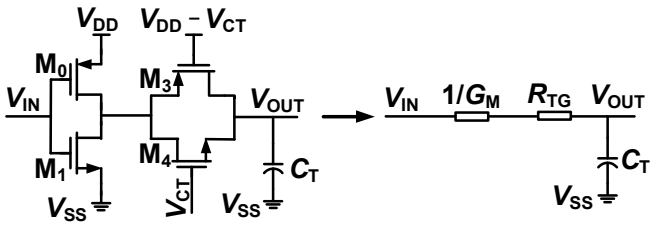

Figure 5. The simple model of delay approximation.

Figure 6 depicts a three-stage VCO utilizing transmission gates, which includes including inverters and transmission gates. The voltage V_{CT} controls the resistance of transmission gates, which affects the delay time of each step. As a result, the frequency of the output signal may be modified.

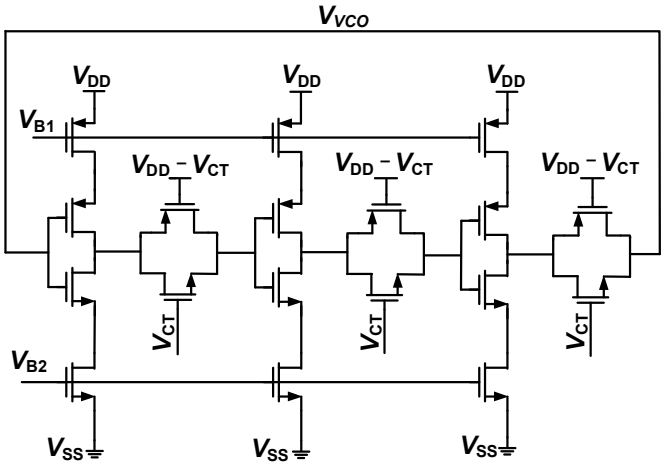

Figure 6. The three-stage VCO using transmission gates

2.3. Duty cycle control circuit

The duty cycle control circuit, which works as an inverter with a movable reverse point, consists of two inverters connected in parallel with two inputs, one as a signal from the oscillator and the other as the duty cycle control voltage V_{DT}. Another inverter is added to refine the signal after the transformation. The circuitry is depicted in Figure 7. Suppose all transistors operate in a saturate region, the voltage V_{BUFF} can be calculated as (6) where r is ON resistance of MOS transistor.

$$V_{BUFF} = V_{DD}.\frac{r_6 \parallel r_8}{r_5 \parallel r_7 + r_6 \parallel r_8} \quad (5)$$

V_{BUFF} is determined by the ON resistances of M_7 and M_8, which are regulated by V_{DT}. Therefore, the duty cycle control voltage V_{DT} can change the duty cycle of the output signal by moving the reverse point of the inverter formed by M_5 and M_6 [2].

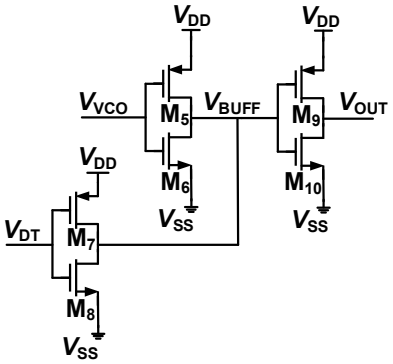

Figure 7. Duty cycle circuit

3. RESULTS AND DISCUSSION

The whole system is designed and simulated by a process of 90nm CMOS technology. Figure 8 shows the layout of the proposed VCO which occupy an active chip area of 0.078mm^2. The oscillating frequency versus the control voltage V_{CTRL} is shown in Figure 9. In case V_{CT} is lower than 0.6V, the signal output of the oscillator remain unchanged. Otherwise, the frequency of the VCO's output signal increases up to 1.7GHz at V_{CT} = 1.8V. Figure 10 shows the duty cycle adjusted result at 3 representative frequencies. The duty cycle of output signal was adjusted linearly from 20 - 80%. Table 1 shows the comparison table of parameters of other architect op-amps.

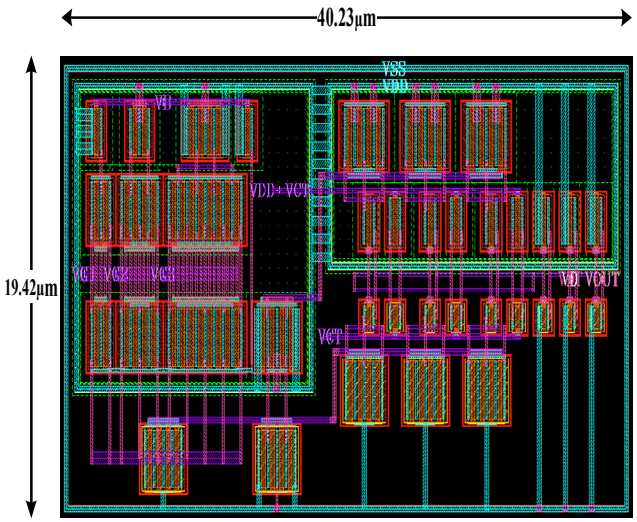

Figure 8. Layout of the proposed circuit

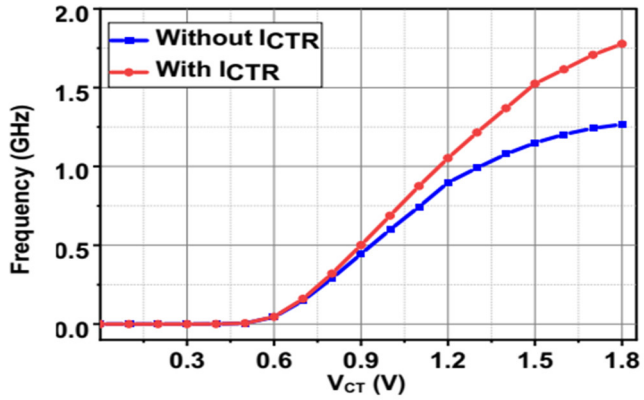

Figure 9. VCO oscillating frequency

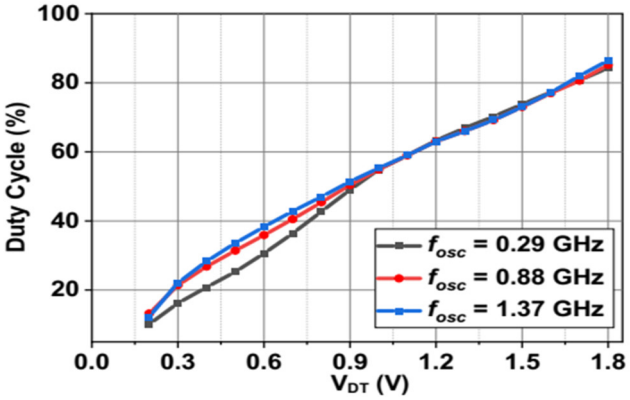

Figure 10. Output duty cycle adjustment range

Table 1. Summary results of the proposed VCO

	[5]	[3]	[2]	This work
CMOS Technology	350nm	180nm	180nm	90nm
Power supply (V)	3.3	3.3	1.5	1.8
Max. frequency	260MHz vs V_{CT}=3.3V	368.9MHz vs V_{CT}=3.3V	1.4GHz vs V_{CT}=1.5V	1.77 GHz vs V_{CT}=1.8V
Min. frequency	17.1Hz vs V_{CT}=0V	16MHz vs V_{CT}=1V	300Hz vs V_{CT}=0V	100Hz vs V_{CT}=0V
Kvco	105.27MHz/V	153.43MHz/V	1.38GHz/V	1.41GHz/V

4. CONCLUSION

A new design of ring oscillator based VCO is proposed. The proposed design allows implementation of a voltage-controlled ring oscillator with wide tuning range and fast voltage swing. The simulation results using CMOS 90nm technology show that the frequency can be tuned up to 1.77GHz and the duty cycle can be adjusted in wide range 20 - 80% independently from the oscillating frequency. Furthermore, the maximum oscillation frequency of the proposed circuit depends on the device sizes. The proposed circuit is applicable for a lower supply voltage because of its simple structure.

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THÔNG TIN TÁC GIẢ

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