SIMULATION AND MODELING OF A 13-BIT SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTER

MÔ PHỎNG VÀ MÔ HÌNH HÓA BỘ CHUYỂN ĐỔI TƯƠNG TỰ - SỐ 13-BIT SUCCESSIVE APPROXIMATION REGISTER

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ABSTRACT

This paper presents the proposed modeling of a 13-bit auto-configurable successive approximation register analog digital converter (SAR-ADC) used for biomedical industry applications. With a Matlab model, the proposed SAR-ADC uses the non-ideal switching to an ideal ADC model, therefore, the non-ideal circuitry implemented at the transistor-level as in the conventional methodology can be isolated. The SAR ADC blocks are modelled according to how the ADC works in voltage mode or current mode and under non-ideal cases such as the effects of clock jitter and noise. Thanks to the above advantages, the behavioral modeling method allows the designer to create an environment to give the most accurate electrical and dynamic parameters. With 13-bit SAR ADC, this paper has measured performance parameters as signal-to-noise ratio (SNR) as high as 79.96dB, effective numbers of bits (ENoB) of 12.98 bits with the spurious-free dynamic range (SFDR) of only 101.16dB.

Keywords: *Analog-to-digital converter, behavioral modeling, successive approximation register.*

TÓM TẮT

Bài báo này trình bày mô hình được đề xuất của bộ chuyển đổi tương tự-kỹ thuật số xấp xỉ 13 bit có thể cấu hình tự động (SAR-ADC) được sử dụng cho các ứng dụng ngành y sinh. Với mô hình Matlab, SAR-ADC được đề xuất sử dụng chuyển mạch không lý tưởng sang mô hình ADC lý tưởng, do đó, có thể tránh những thành phần không lý tưởng của mạch được thực hiện ở mức transistor như trong phương pháp thông thường. Các khối SAR-ADC đã được mô hình hóa theo cách ADC hoạt động ở chế độ điện áp hoặc chế độ dòng điện và trong các trường hợp không lý tưởng như ảnh hưởng của sai lệch xung nhịp và nhiễu. Nhờ những ưu điểm trên, phương pháp mô hình hóa hành vi cho phép người thiết kế tạo ra môi trường để đưa ra các thông số điện và động lực học chính xác nhất. Với SAR-ADC 13-bit, bài báo này đã đo các thông số hiệu suất như tỷ lệ tín hiệu trên nhiễu (SNR) cao tới 79,96dB, số bit hiệu dụng (ENoB) là 12,98 bit với dải động không có nhiễu (SFDR) là chỉ 101,16dB.

Từ khóa: *Bộ chuyển đổi tương tự sang số, mô hình hóa hành vi, thanh ghi xấp xỉ liên tiếp.*

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1. INTRODUCTION

Portable biopotential sensing applications requites low-power consumption for long battery life. The neural signals such as Electrocardiogram (ECG) and Electroencephalogram (EEG) have a bandwidth from sub low frequency up to a few kHz [1, 2]. The amplitude of ECG and EEG [3] is about 1mV and from 10 to 100μV, respectively. Thus, biomedical signal must be amplified before signal processing. And following the important block is the analog to digital converter (ADC) for signal processing. Nowadays Successive-Approximation-Register (SAR) Analog-to-Digital-Converter (ADC) is widely used for low power ADC architecture [4-6]. Typically, ADCs model mixed-signal circuits are realized at the operational level and accuracy and take a long time to simulate. Therefore, to perform complex designs, a more accurate and rapid model is needed to validate the algorithms and architecture of the ADC and evaluate their performance parameters. One of such approaches being followed is behavioral modeling [7]. This approach uses the mathematical specification of each of the ADC's building blocks and thus provides a model for analysis and synthesis based on the desired specifications. In the context of ADCs, the choice of architecture mainly depends on its performance parameters, such as sampling rate, resolution, signal-to-noise ratio (SNR), level of power consumption, etc. This paper focuses on the next approximation register (SAR) ADC due to its small operating area and minimal operational requirement of analog components while achieving low power consumption [8].

This paper presents the behavioral model of SAR-ADC implemented in the Matlab simulink. The SAR-ADC simulink uses the non-ideal switching model instead of the non-ideal circuitry implemented at the transistor level as in the usual methodology for modeling sampling jitter, noise, etc. With 13-bit SAR ADC, the design has achieved performance parameters such as signal-to-noise ratio (SNR) as high as 79.96dB, effective numbers of bits (ENoB) of

12.98 bits with the spurious-free dynamic range (SFDR) of only 101.16dB.

2. PROPOSED MODEL SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTER

The SAR ADC basically performs a binary search in a set of all quantum levels before exporting the final result. Figure 1 shows the proposed block visual of a 13-bit SAR ADC which consists of a sample and hold (S/H) for sampling and holding the analog input signal in a specific period of time. A comparator block is used to compare the sampled analog value (V_{IN}) with the analog signal from the digital-to-analog-inverter (DAC) block corresponding to 13-bit and generate a comparison signal accordingly as logic "1" or "0". The SAR block is utilized for controlling logic for generating the digital data from the most significant bit (MSB) D_{12} with regard to the least significant bit (LSB) D_0 by sequentially approximating the digital n-bits as per the comparator output and n-bit DAC to produce an analog value corresponding to the digital data from the SAR block. The SAR includes output registers to save data. It consists of an additional clock generator that gives the ADC an internal clock. In this paper, input signal indicating the start of conversion (SC) and output signal indicating the end of conversion (EOC).

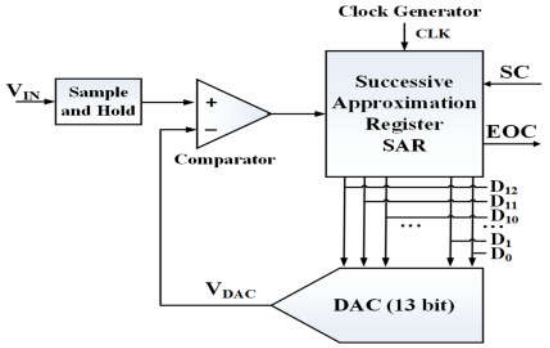

Figure 1. Block diagram of the proposed 13-bit successive approximation register ADC

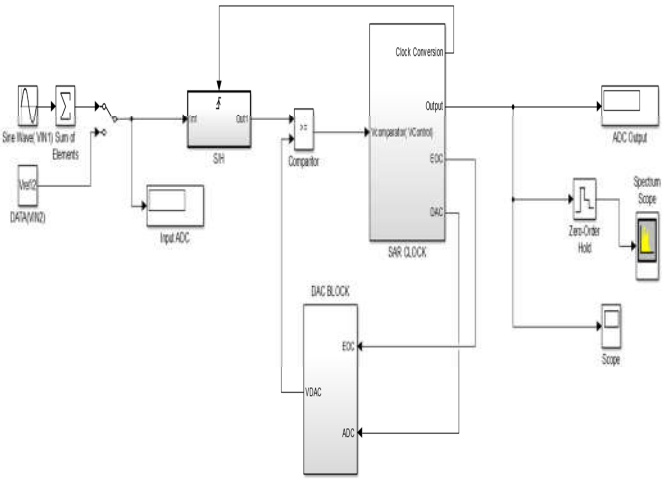

Figure 2. Proposed model of the 13-bit successive approximation register ADC

Figure 2 shows the model of the proposed auto-configurable SAR ADC which is a typical set of SAR ADCs consisting of a configuration unit used to provide clocks and sampling clocks depending on the type of input signal. The input signal referred to here can be cardiac or neural. The heart and nerve implanted analog inputs are fed to the configuration device and the S/H circuit. Now in the SAR, an additional serial digital data bus is used to convert the engineering data parallel digital data to serial digital data. When analog input V_{IN} is put into the S/H block. S/H is a critical block of the ADC and it samples the external analog input signal and holds the input stable for a certain period of time so that it can be converted into digital form.

The DAC in this work does not include a comparator and sampler as showed in Figure 3. The non-ideal DAC is essentially a series of binary capacitors (the capacitance increases exponentially by a multiplier of 2) and the associated switch completely different from the ideal DAC' blocks that are shown in Figure 4. While the upper plates of the capacitor are switched on/off into the input signal and the lower plates are initially connected to a common voltage V_{CM} which is then switched to one of two reference voltages. Switching the top plate of the capacitor is taken care of by the keys in the sampler, so the DAC consists of a binary capacitor bank and 3-point locks connected to the common level or two reference voltages as presented in [9]. The DAC performs comparator voltage generation (the voltage across the capacitor plates) from the feedback bits from the SAR register through varying the lower plate voltage of the capacitors. Binary capacitors and 3-point junction locks have been covered a lot, so we won't go into this section in depth. The SAR ADC architecture is one of the most popular architectures in use today. The simplicity of the design allows the SAR ADC to achieve high speed and resolution while maintaining a relatively small footprint and power consumption. The accuracy limit of the SAR ADC depends mainly on the accuracy of the DAC. If the DAC does not give the correct standard voltage levels to compare with the input signal, the output of the converter will be wrong so in this DAC block we improve and simulate to match the SAR ADC 13-bit.

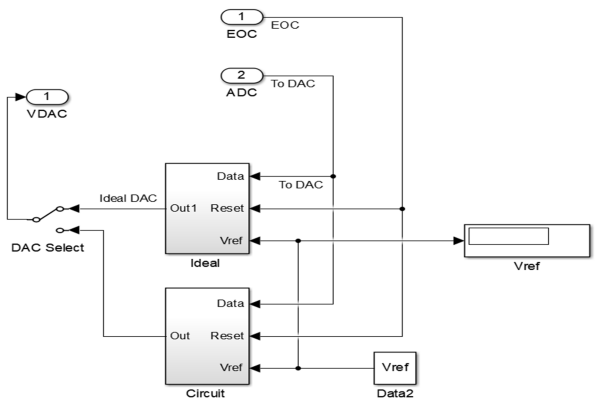

Figure 3. Block diagram of the DAC

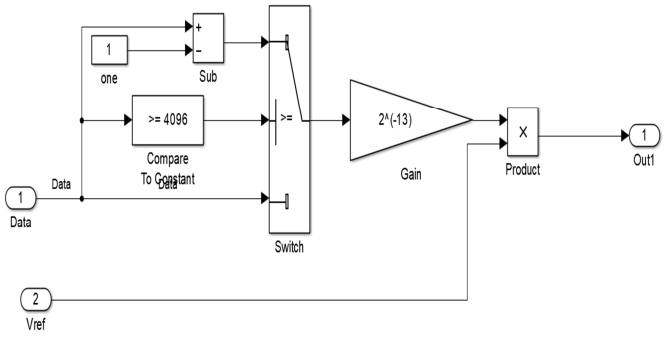

Figure 4. Block diagram of Ideal DAC

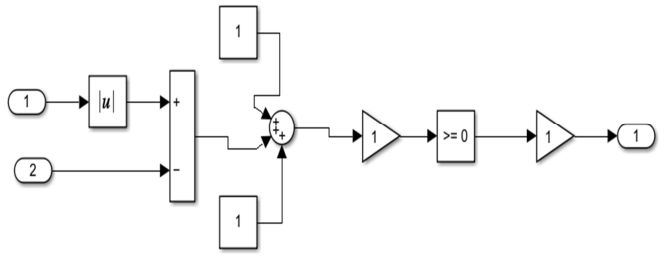

Figure 5. Block diagram of the ideal comparator

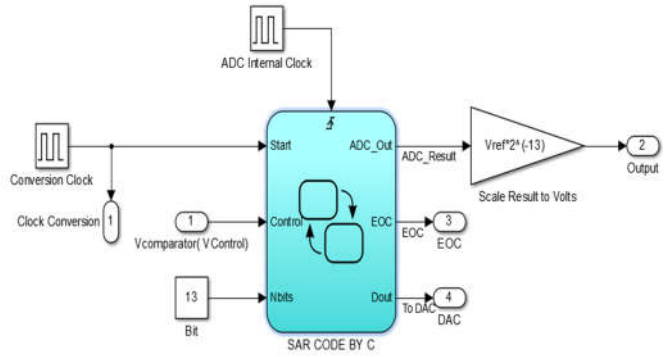

Figure 6. Operation diagram of 13-bit SAR ADC block

The comparator is one of the important building blocks of the SAR ADC and needs to resolve the difference between the two signals in the accuracy of the system while maintaining its speed. It is a link between the analog and digital fields and is therefore considered a non-linear analog device. The proposed ideal comparator behavior model is shown in Figure 5. A comparator block is used to reduce power dissipation as presented in [10]. The purpose here is to compare the input voltage with the V_{DAC}. V_{IN} sample and input are kept and subtracted from V_{DAC}, the analog output signal of the DAC corresponding to n bits is generated sequentially, and the output is amplified by the amplifier stage. The result is then fed into a block that compares to 0 to determine which input is higher. Figure 6 shows the SAR architecture which consists of a Conversion Clock and ADC Internal Clock block. The Conversion Clock operates when the SAR DAC performs a bitwise MSB to LSB comparison, and the ADC Internal Clock operates when the bit comparison cycle in the SAR ADC is done. The sampling control technique generated by the SAR is used to enable the sampling block and hold and store the analog input signal. The sampling block suffers from non-linear distortion and thermal noise as introduced in [11]. Distortion is modeled using generic function blocks, and in this set of SARs, we graphically represent the register login of approximately ten consecutive bits using the C and Matlab programming languages.

The comparator and the Sample and Hold unit are ideal components in the circuit. For holding and sampling circuits, use ideal circuits to avoid quantization errors, jitter errors, flicker noise and thermal noise. The purpose of the ideal comparator here is to compare the input voltage with V_{DAC}. In analog-to-digital converters, the main sources of consumption are the digital control circuits and the capacitive DAC array. While the power consumption of the digital converter circuitry has benefited from the development of technology, the power consumption due to the capacitive array is limited by the mismatch of the capacitor and is independent of the technology. Therefore, the DAC topology and switching algorithms are proposed to reduce DAC power and rely on the highly linear characteristics of the binary-weighted network. In fact, with the ideal DAC circuit, the minimum capacitor value provided by the designer is much larger than is needed to satisfy the linearity requirements. This results in a remarkably large array capacitance and high switching power generation. The purpose of this design is to demonstrate that a binary with weighted attenuation capacitor (BWA) can achieve efficiencies below 10fJ/switching step, while the simulation Accurate simulation and modeling with custom capacitors.

3. RESULTS AND DISCUSSION

The proposed 13-bit SAR ADC is in essence configurable, and the main component of the proposed configuration unit is its frequency detection unit, which determines the frequency of the input analog signal, based on the operating clock frequency and sample rate of the selected ADC. To confirm the proposed behavioral model of the ADC and understand the effects of various non-ideal things, the proposed ADC was simulated for the desired specifications. The original input signal is implanted and the output waveforms of the signal are reconstructed using the proposed ideal and non-ideal 13-bit configuration SAR ADC. Figure 7 shows the analog input signal at frequency of 10MHz with a V_{PP} = 3V. Figure 8 shows the SAR-ADC's output signal when the DAC is case of ideal. While Figure 9 shows the SAR-ADC's output signal when the proposed DAC approach is applied. Beside we also achieve that the ideal DAC achieves an SNR as high as 80.02dB, which equates to an effective bit count (ENoB) of 13-bit, in the non-ideal case, an SNR of 79.96dB and an ENoB of 12.98-bit are achieved. In addition, the non-ideal DAC has -78.73dB lower distortion (total harmonic distortion - THD) than the THD of the non-ideal DAC. The spurious-free dynamic range (SFDR) and signal-to-noise and dis`tortion ratio (SINAD) is achieved in the ideal case of 101.16dB and 79.91dB.

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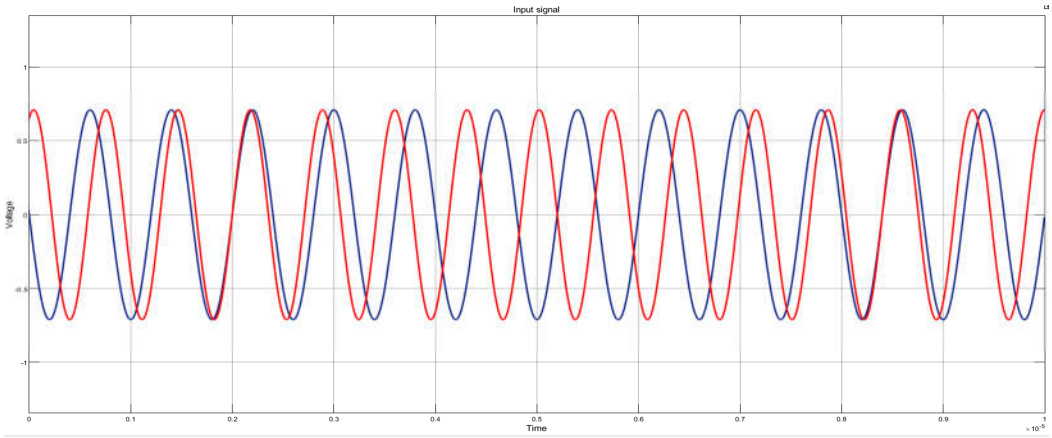

Figure 7. Input analog signal

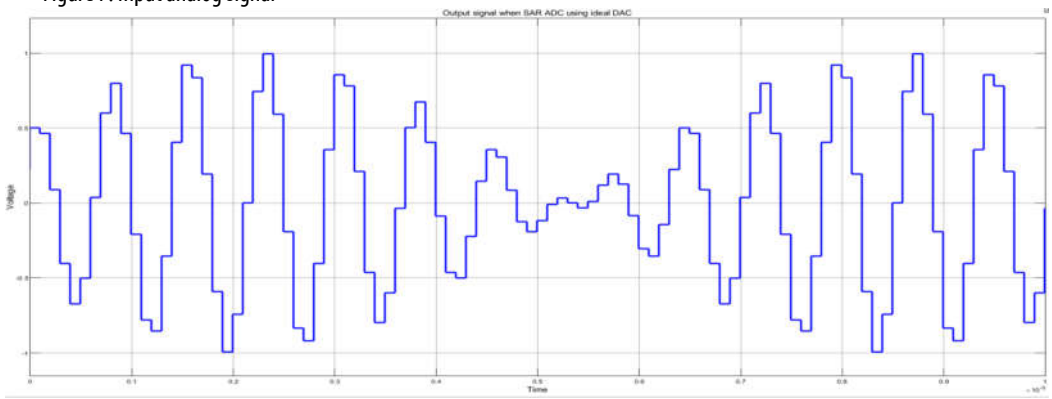

Figure 8. Output signal of SAR ADC's block with ideal DAC's block

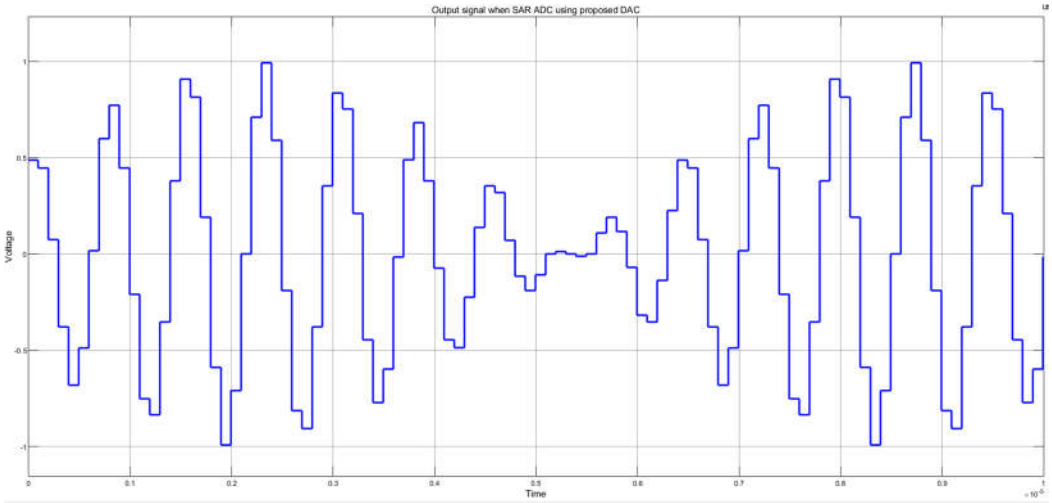

Figure 9. Output signal of SAR ADC's block with no-ideal DAC's block

Table 1. Performance summary and comparison

Architecture	[12]	[13]	[14]	This work
Sampling rate (MS/s)	180	180	300	140
Frequency (MHz)	200	10	19.63/146.19	10
Binary weighted with attenuation capacitor	Yes	No	No	Yes
Bit	13	12	12	13

The input of the analog signal is held and sampled through the Sample and Hold a unit and then passed through the comparator that is compared to the output of the DAC's block. Here, the successive approximation converter essentially performs a binary search in the set of all quantile levels before outputting the final result. A shift register is responsible for controlling the operation of the ADC. The output of the comparator controls the binary search, and the output of the next approximation register is the result of the conversion. Through conversion steps, the analog signal is converted to a digital signal. Because of the different quantization levels, the output of the signal will have different orders. The output signal of the SAR ADC with the use of the proposed DAC block has approximately the same quantization orders and levels as the output signal when using the ideal DAC. Table 1 shows some optimization parameters of this paper compared to other articles.

4. CONCLUSION

This paper presents a novel behavioral model of an auto-configurable 13-bit architecture of SAR ADCs for possible use in cardiac transplantation and neuroendocrine applications, acquisition of various cardiac and nerve physiological signals. The behavioral modeling approach provides independence and fast computation times along with flexibility in introducing various non-ideal factors, such as clock vibrations, clock shifts, thermal noise and flashing on the various building blocks of the SAR ADC. The configurable nature of the ADC is achieved by including a configurable unit in the conventional SAR topology,

selecting the clock and sampling frequency to match the frequency of the input signal. From the simulations, it is observed that the proposed ADC behavioral model achieves an SNR as high as 79.96dB with an ENoB of 12.98 with very low distortion -78.73dB and, with a balance of non-linear factor, very small performance degradation occurs.

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THÔNG TIN TÁC GIẢ

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Khoa Điện tử, Trường Đại học Công nghiệp Hà Nội